

## **Renesas Technology and Hitachi Announce Development of SH-2A 32-Bit RISC CPU Core for High-Performance Embedded Systems**

— Approximately 3.5-fold improvement in processing performance plus improved program code efficiency and real-time capability, ideal for high-performance real-time control systems for automotive, consumer, and industrial products —

Tokyo, April 19, 2004 — Renesas Technology Corp. and Hitachi, Ltd. (TSE:6501, NYSE:HIT) today announced the development of a 32-bit RISC (Reduced Instruction Set Computer) CPU core, dubbed the SH-2A, for use in control devices in the automotive, industrial, and consumer fields.

The SH-2A is the successor of the SuperH™\*<sup>1</sup> RISC microprocessor SH-2 CPU core, and offers a major increase in performance together with improved program code efficiency. The SH-2A is designed for products requiring real-time capability, and is ideal for use in single-chip microcontrollers and SoCs (Systems on Chip) in automotive engine control systems and consumer and industrial products such as printers and AC servos.

### **< Background >**

Automotive engine control has become more complex with the recent emphasis on environmental conservation and improved fuel consumption, while at the same time there is a trend toward the development of large-scale systems in short time-frames through the adoption of autocode technology\*<sup>2</sup> driven by improvements in development tools. The field of industrial products such as AC servos is also witnessing advances in system precision, while more and more consumer products such as printers are appearing in the form of multi-function systems. For example, there is a demand for faster processing providing coupled printing control while executing high-speed computational operations on image data from a DSC or scanner, and control system in these fields require microcontroller that offer high speed, high performance, and large-capacity on-chip ROM.

Against this backdrop, Renesas Technology has to date released single-chip microcontrollers for these markets featuring an SH-2 32-bit RISC CPU core with an operating frequency range of 50 MHz to 80 MHz, together with on-chip peripheral functions including fast, large-capacity flash memory, a 16-bit PWM timer, and A/D converter, which are currently widely used.

Now, in response to the need for even higher speed and performance, Renesas Technology and Hitachi have jointly developed the new SH-2A RISC CPU core as an upward-compatible version of the SH-2. Features and details of the SH-2A are as follows.

-more-

## < Features and Details >

- (1) Use of superscalar architecture\*<sup>3</sup> and Harvard architecture\*<sup>4</sup>

Use of a superscalar architecture, a kind of CPU core instruction processing architecture, enables up to two instructions to be executed simultaneously. In addition, a Harvard architecture is employed that uses separate data buses for data and instructions, preventing contention between instruction fetches and data accesses. As a result, performance does not degrade when executing operations involving consecutive memory accesses.

- (2) High processing performance of 360 MIPS (million instructions per second) at 200 MHz operation

The current SH-2 has a processing performance of 104 MIPS at the maximum operating frequency of 80 MHz, while the SH-2A achieves processing performance of 360 MIPS at 200 MHz — an approximately 3.5-fold improvement.

Processing performance per 1 MHz unit frequency has been improved approximately 1.4-fold, from 1.3 MIPS to 1.8 MIPS, through the use of a superscalar architecture. In other words, an approximately 40% improvement in performance is achieved at the same operating frequency, and a lower operating frequency is required to achieve the same performance, enabling system power consumption to be reduced.

- (3) New instruction set and improved code efficiency

The instruction set of the SH-2A is upward-compatible with that of the SH-2. New 32-bit instructions and addressing modes have been added to the previous 16-bit instructions, and a total of 112 instructions are now supported, including 21 FPU (floating-point processing unit) related instructions.

Addressing modes using 32-bit instructions enable program address information, etc., to be embedded in the instruction code, making it possible for a larger area to be accessed by a single instruction. This enables program code to be made smaller than in the case where address information is stored in memory in table form, as at present, reducing the necessary memory capacity and so helping to cut system costs.

In addition, the SH-2A supports the following instructions offering improved real-time control performance and code efficiency.

- (a) Bit-operation instructions that improve real-time performance
- (b) Instructions offering faster, single-instruction implementation of 32-bit data division
- (c) Barrel-shift instructions enabling shifting of any number of bits
- (d) Store-multi/load-multi instructions enabling single-instruction coding of stack save/restore operations for CPU general registers required in the event of a subroutine call

The instruction set is upward-compatible with that of the SH-2, enabling programs developed for the SH-2 to be used as a further aid to reducing system development time.

- (4) Fast application program switching in case of interrupt events

Normally, when an interrupt event occurs, CPU internal register information at that point is stored in stack memory by software processing before execution of the application program for the interrupt event is started.

The SH-2A incorporates special-purpose registers for storing CPU internal register information. The CPU and special-purpose registers are connected via a dedicated bus, and when an interrupt event occurs, CPU internal register information is stored in the special-purpose registers at high speed by hardware.

As a result, the time between the occurrence of an interrupt event and the actual start of application program execution has been cut from a minimum of 37 cycles in the SH-2 to 6 cycles in the SH-2A. This enables fast application program switching to be implemented, making it possible to achieve high-quality real-time control with better responsiveness.

Development tool plans include the development of an SH-2A C/C++ compiler, and support of the compact E10A-USB, and the E200F incorporating a real-time profiler function, as emulators.

Renesas Technology plans to release an initial-phase product incorporating the SH-2A by the third quarter of 2004, and to continue with subsequent phased releases.

- Notes: 1. SuperH is a trademark of Renesas Technology Corp.
2. Autocode technology: A technology for automatically generating software from a block diagram or state machine, without the need for actual C-language coding.
  3. Superscalar architecture: A method of increasing the processing speed of a computer by simultaneously executing multiple instructions in one clock cycle.
  4. Harvard architecture: An architecture that uses separate data buses for instructions and data, enabling instruction fetches and data accesses to be executed simultaneously.
- \* Other product names, company names, or brands mentioned are the property of their respective owners.

#### < Typical Applications >

- Automotive applications: Engine control systems, body control systems, etc.
- Consumer products: Printers, DVD recorders, etc.
- Industrial equipment: AC servos, general-purpose industrial inverters, etc.

#### < Specifications >

| Item                   | Specifications  |
|------------------------|---|
| CPU core name          | SH-2A   |
| Number of instructions | 112 (including 21 FPU-related instructions) <Upward-compatible with SH-2> |
| Processing performance | 360 MIPS, 400 MFLOPS (at 200 MHz operation)                               |
| Pipelining             | Five-stage  |
| Bus architecture       | Harvard architecture (separation of instructions and data)                |
| Instruction issuance   | Superscalar architecture (simultaneous issuance of 2 instructions)        |

---

Information contained in this news release is current as of the date of the press announcement, but may be subject to change without prior notice.

---