MEGA-CD SOFTWARE DEVELOPMENT MANUAL

REX SATO

SEGA ENTERPRISES, LTD.

VER. 0.10 3/6/91

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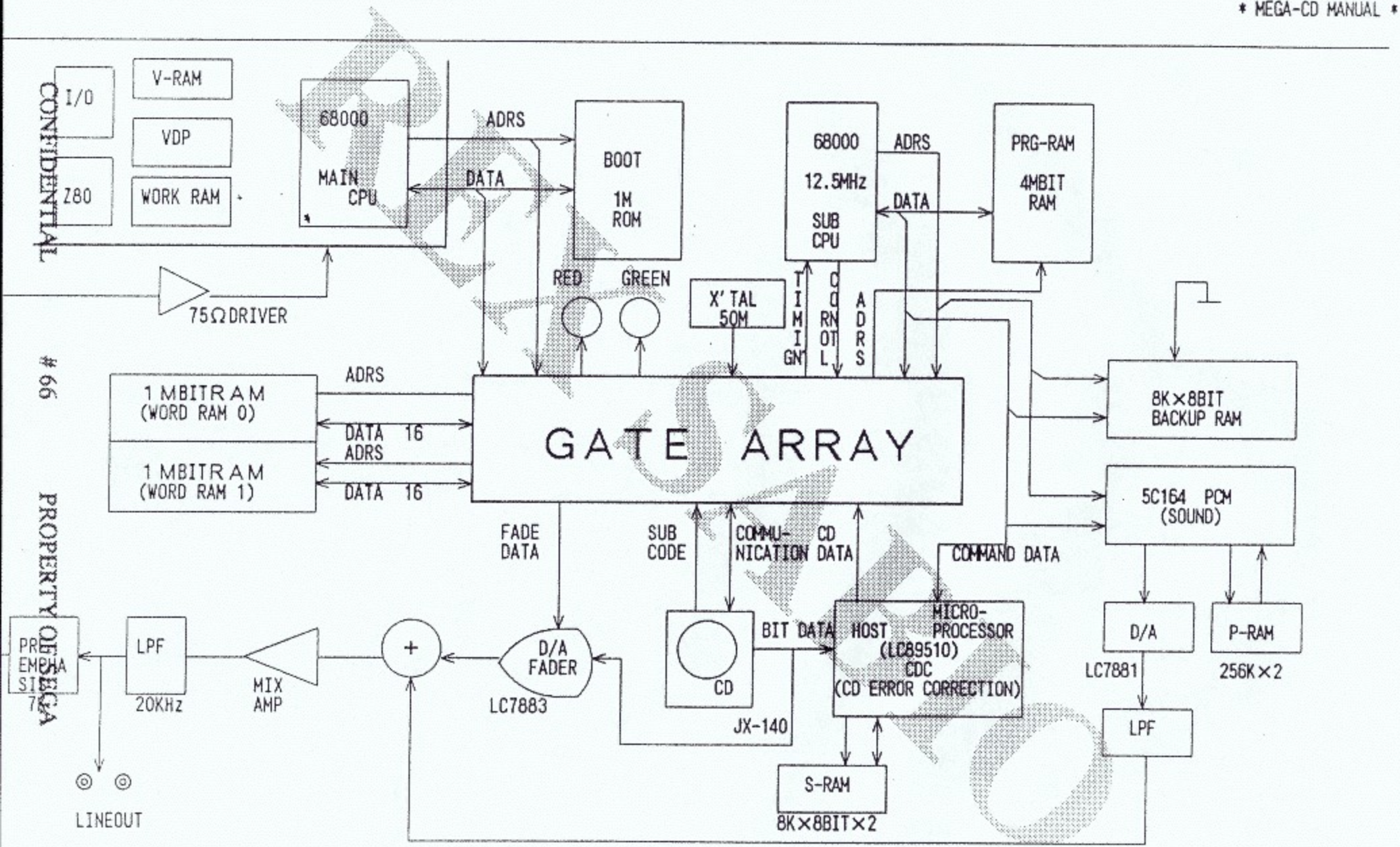

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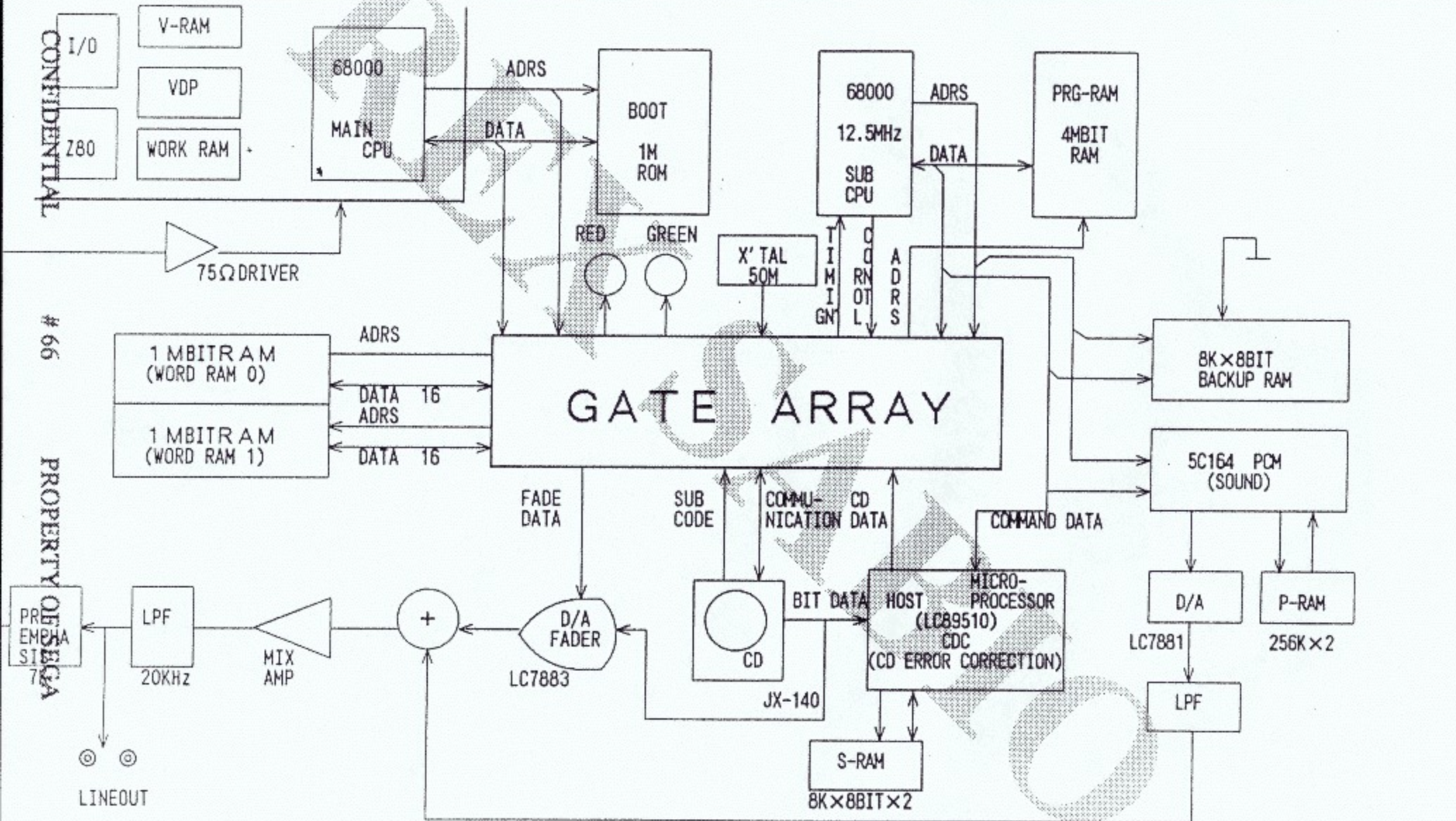

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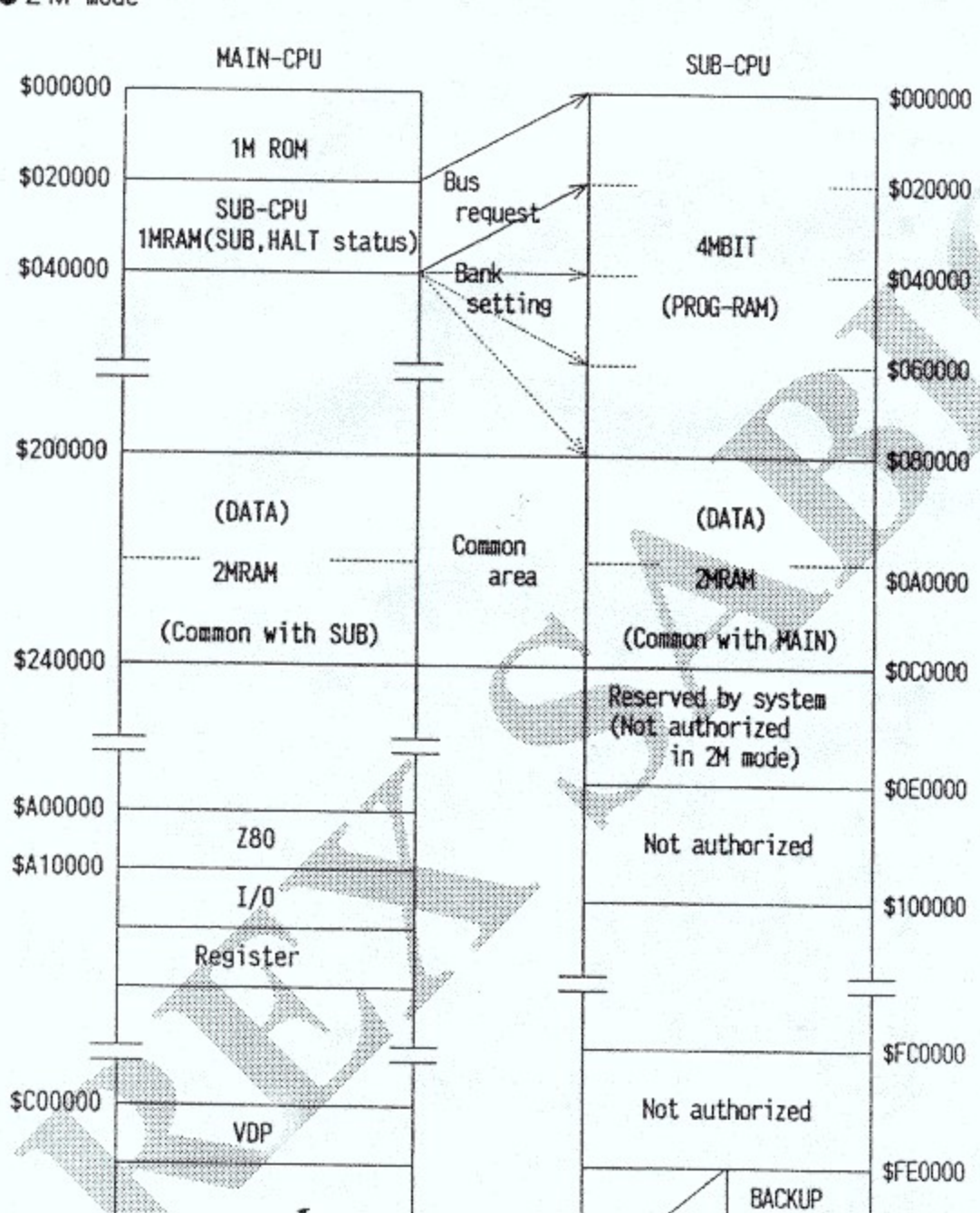
RETSABIO

1. MAPPING

● 2M mode



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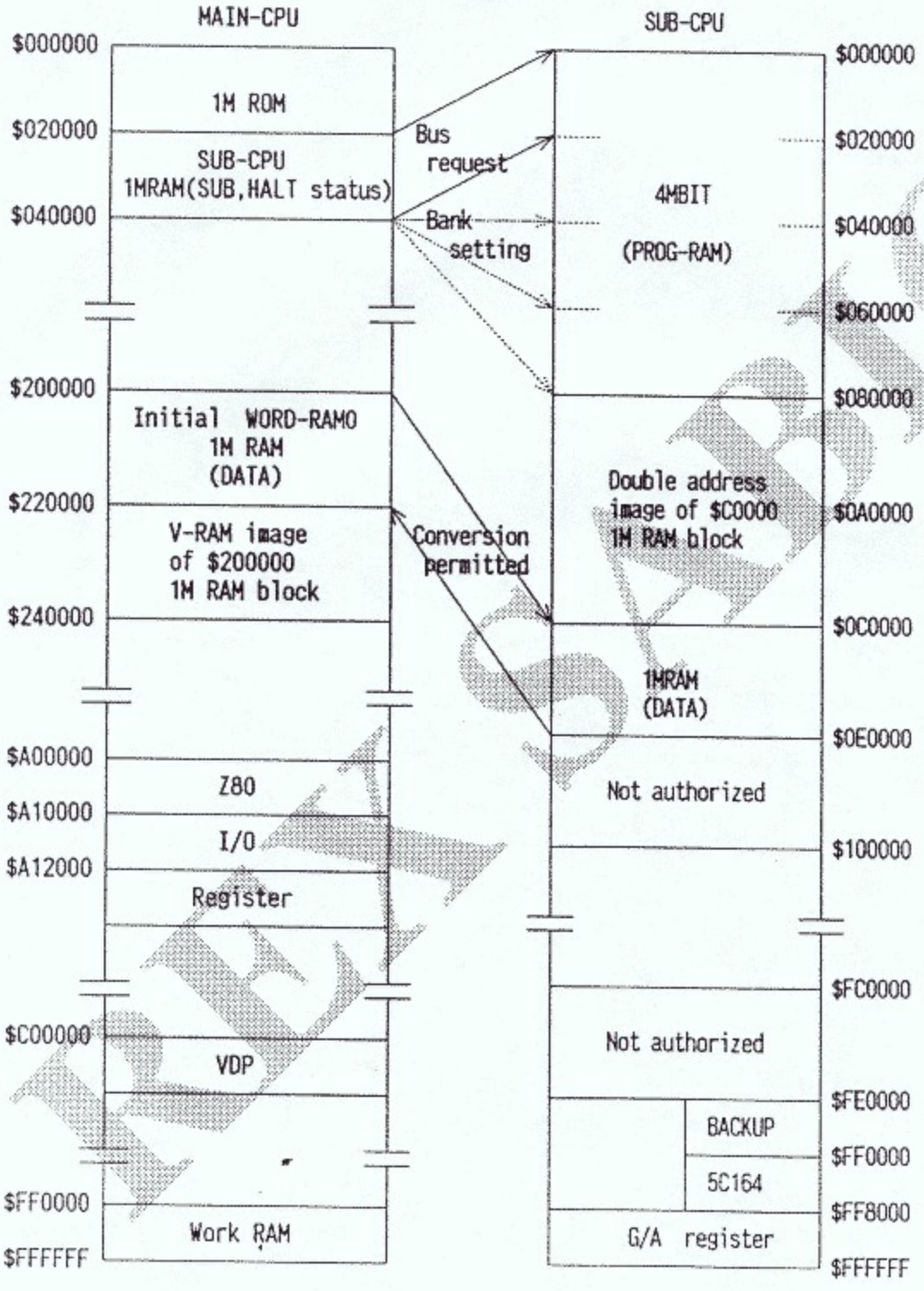
● 1 M · 1 M mode



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2. MAIN CPU MAPPING

●$000000~$01FFFF

CD-ROM boot memory.

●$020000~$03FFFF

By sending a HALT signal to the SUB-CPU, the sub-CPU PRG-RAM (1M) can be used for data reads/writes from the MAIN-CPU.

●$040000~$1FFFFF

Reserved by system.

●$200000~$23FFFF

Also refer to the description of register $0ff8002 regarding this block.

(1) 2M mode, ($FF8002 BIT 2 MODE=0)
Used by switching the same word RAM back and forth with the SUB-CPU.
This is the mode at power-on, and this block is assigned as word RAM.

(2) 1M mode, ($FF8002 BIT 2 MODE=1)
$200000-$21FFFF; Word RAM either 0 or 1.
$230000-$23FFFF; When the above 1M bitmapped image data is written to this area, the VDP cells are arranged vertically and DMA is used to transfer data using the appropriate sequence of address number.

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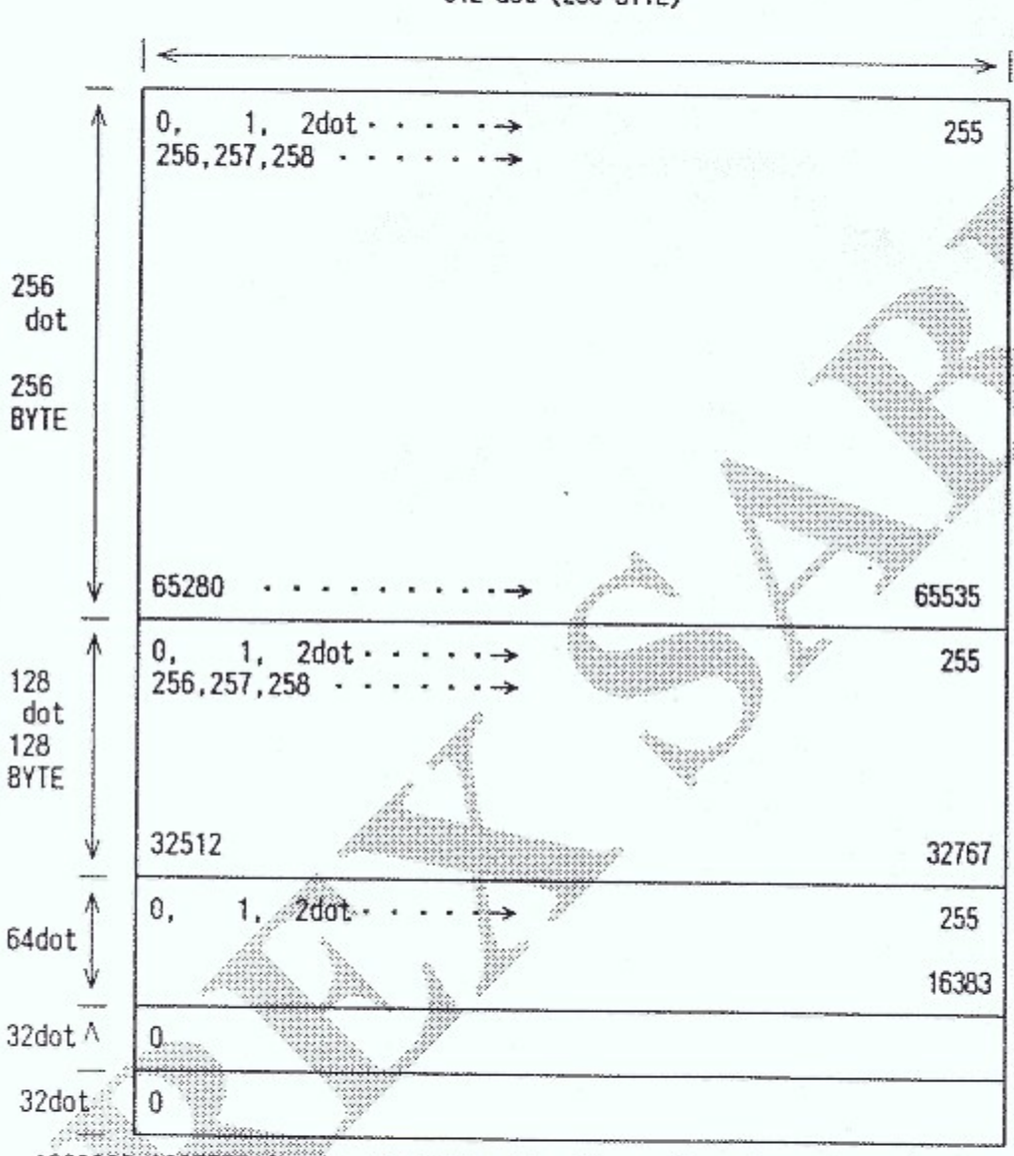
By setting $200000-$21FFFF word RAM to either 0 or 1, bitmapped images can be created as shown below. Three screen sizes are available, 512 horizontal dots (fixed) by either256, 128 or 64 vertical dots. There are two 64-dot modes. Each dot is composed of 4 bits. (bits 7-4 compose dot 0, bits 3-0 compose dot 1,etc.).



$220000-$23FFFF is the area where the data written above is read as a V-RAM image. If the data is read out in the sequence 0, 1, 2, 3, 4, 5, 6, 7, 256, 257.....263, 512, 513.....519....., it can be read in the same manner as when the VDP cells are arranged vertically. When 65287 is reached, the next cell begins, this time using the sequence 8, 9, 10, 11, 12, 13, 14, 264, 255 ... 271, 520 .....

The number of cells is determined by the 1M addresses.
32cell: From $220000
16cell: From $230000
8cell: From $238000
4cell: types, from $23C000 and from $23E000

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●$240000~$A1FFFF

Refer to the MD manual for information on this address space.

●$A12000~$A1202F

See the description of the main CPU registers.

●$A12030~$FFFFFF

Refer to the MD manual for information on this address space.

3. SUB-CPU MAPPING

●$000000~$01FFFF : PROGRAM RAM.

(1)SUB-CPU program
(2)CD TOC data
(3)PCM(RF%C!&$) data

At system startup the SUB-CPU program data is transferred to this memory area from the main CPU. Also, an area of fromo $0-$0FEFF starting at $A12002 of the main CPU can be write protected in 100H units.

●$020000~$07FFFF : Reserved by system.

●$080000~$0BFFFF :Data RAM

(1)2M mode, ($FF8002 BIT 2 MODE=0)
This RAM area is used for rotation compression (axis conversion). It is related to registers $FF8058 through $FF8066. It can of curse also be used as normal RAM.

(2)1M mode, ($FF8002 BIT 2 MODE=1)
When full graphic images are developed in 1M of RAM, the data is handled 1 bit per dot. In this 2M area, bits 4-7 and bits 12-15 of the 16bit data are invalid. They are output as 0s when the data is read. Byte writing (bits 0-7 and 6-15) to this area is supported. The area to which data is actually written is $0C0000-$0DFFFF.

●$0C0000~$0DFFFF : Data RAM

(1)2M mode, ($FF8002 BIT 2 MODE=0)
RAM is not assigned to this ara.

(2)1M mode, ($FF8002 BIT 2 MODE=1)
1M of RAM (called word RAM) is assigned to this area. There are two blocks of word RAM, WORD-RAM0 and WORD-RAM1. They are used for conversion between the main CPU and the SUB-CPU. See the description of register $0FF8002 for details.

●$0E0000~$FDFFFF

Prohibited. (Some parts may be used for intermediate image reads/writes, but as this block may be required later on it should never be accessed!)

●$FE0000~$FE3FFF

The battery pack up RAM 8Kbyte address is the lower byte only.

●$FE4000~$FEFFFF

Reserved by system.
An image of the above battery pack up RAM can be obtained from this area, but is should not be accessed.

●$FF0000~$FF7FFF

This is the PCM sound source address area. Refer to the RF5C164 manual for instructions on how to use it.

●$FF8000~$FF81FF

SUB-CPU register.

●$FF8200~$FFFFFF

Reserved by system.

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4. MEGA-CD REGISTER TABLE

	SUB-CPU $0FF8000	MAIN-CPU $0A12000
00 02	Initialization Ver. No. / Reset / LED Memory mode/Priority/Write protect	Initialization Reset / INT2 Memory mode/ Write protect
04 06 08 0A	CDC (INT5 from LC89510) CDC mode/CDC RS0 CDC RS1 CDC host data (16bit) CDC DMA address	CDC CDC mode H-INT. CDC host data (16bit)
0C 0E 10 ↓ 1E	Communication Stopwatch Communication flag Communication command Word 8 R/W	Communication Stopwatch Communication Flag Communiccaton command Word 8 R/W
20 ↓ 2E	Communiacation status Word 8 R/W	Communication status Word 8 R/0
30	General timer Timer (INT3)	
32	Interrupts INT mask	
34 36 38 ↓ 40 42 ↓ 4A	CDD Fader CDD control CDD status Word 5 (INT4) CDD command Word 5	
4C 4E 50 ↓ 56	Color calculation Font color Font bit Font data Word 4	

SEGA

	SUB-CPU $0FF8000	MAIN-CPU $0A12000
	Rotation compression (2M mode only INT1)	
58	Stamp sizw	
5A	Stamp map base address	
5C	Image buffer V-cell size	
5E	Image buffer start address	
60	Image buffer offset	
62	Image buffer H-dot size	
64	Image buffer V-dot size	
66	Trace vector base address	
	Subcodes	
68	Subcode address	
6A		
↓	Reserved by SEGA	
FE		
100	Subcode	
↓	Data	
17E	(INT.6)	
180	Subcode	
↓	Data	
1FE	Image	

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5. SUB-CPU REGISTERS

●$OFF8000 Reset

MSB LSB

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	LEDG	LEDR	Ver3	Ver2	Ver1	Ver0	–	–	–	RES0
RD	0	0	0	0	0	0	0/1	0/1	0	0	0	0	0	0	0	0/1
WR	0	0	0	0	0	0	0/1	0/1	0	0	0	0	0	0	0	0/1

RES0: Peripheral reset.
Write: '0'=reset, '1' does nothig.
Read : Switched to '1' by hardware after 100ms, indicating that operation is possible.
'0' during reset.

LEDR: Red LED control: '1'=on, '0'=off (access)
LEDG: Green LED control: '1'=on, '0'=off (ready)
Ver.0-3: Indicates the chip version.

Green	Red	CPU and CDD operation (set in software)
0	0	CD not in use or power off
0	1	SEGA RESERVED
1	0	CD ready ... CD loaded (if TOC is readable)
1	1	CD ACCESS
0	0/1	SEGA RESERVED
1	0/1	CD READY ... No CD loaded or until reading of TOC
0/1	0	STANDBY MODE
0/1	1	SEGA RESERVED
0/1	0/1	SEGA RESERVED

0/1 indicates flashing on and off.

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●$OFF8002 : Memory mode

MSB LSB

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
	WP7	WP6	WP5	WP4	WP3	WP2	WP1	WP0	—	—	—	PM1	PM0	MODE	DMNA	RET
RD	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0	0	0	0/1	0/1	0/1	0/1	0/1
WR	0	0	0	0	0	0	0	0	0	0	0	0/1	0/1	0/1	0	0/1

PM0,PM1 : Priority mode 0,1

PM1	PM0	Operation
0	0	Mode OFF
0	1	Write down mode
1	0	Write up mode
1	1	Prohibited

Selects either write down or write up mode when writing from the SUB-CPU to the word RAM double address image in the 1M mode.

In the 2M mode, data from the stamp map can be written to the image buffer using either write down or write up mode, but as the writeing is time consuming real time display is not possible. The best that could be accomplished would be like just drawing the trees for the golf game.

MODE:RAM mode
'0'=2M mode, '1'=1M mode

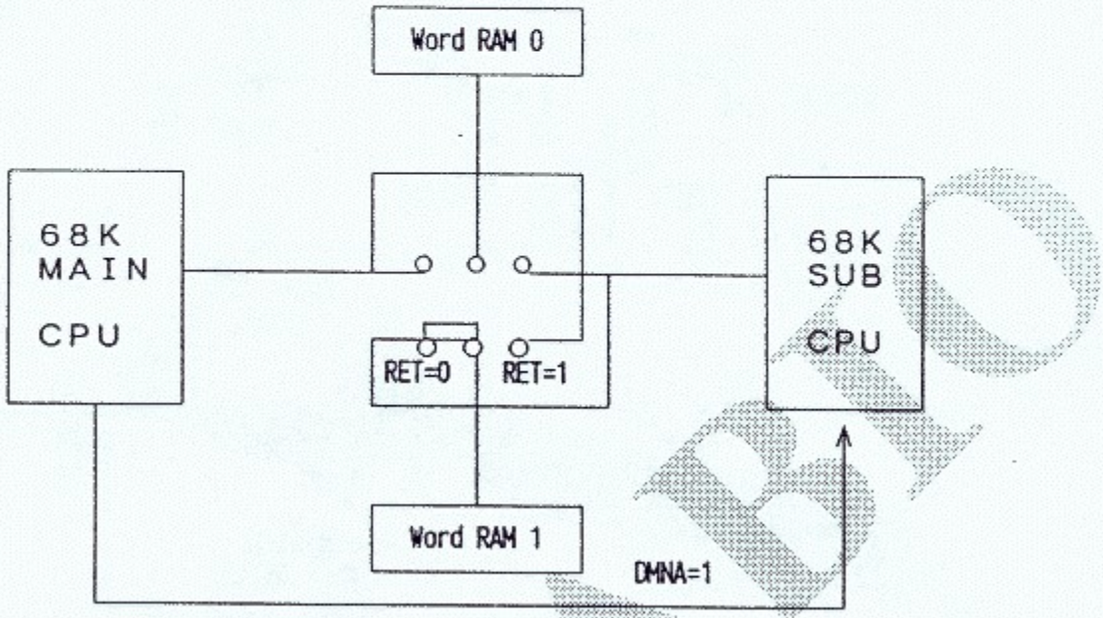
DMNA : Declaration of MAIN-RAM No. Accsess
Mode='0' (2M mode)
Declaration bit that specifies that the main CPU will not access the 2M main RAM area.
When set to '1' the 2M RAM area is assigned to the SUB-CPU.
When set to '0' it is assigned to the main CPU.

Mode='1' (1M mode)
Setting this bit to '1' indicates that a swap request has been made to the SUB-CPU.
When the swap is finished it is reset to '0' by the hardware.

RET : RET bit
Mode='0' (2M mode)
In contrast to DMNA, this is the bit returns the 2M RAM area to the MAIN-CPU.
When set to '1' the 2M RAM area is returned to the main CPU.
When set to '0' it is assigned to the SUB-CPU.
Mode='1' (1M mode)
'0' = WORD-RAM0 assigned to main CPU and WORD-RAM1 assigned to SUB-CPU.
'1' = WORD-RAM1 assigned to main CPU and WORD-RAM0 assigned to SUB-CPU.

WP0-7 : Allows conformation of the addresses write protected by the main CPU. The SUB-CPU range $0-$0FEFF can be write protected in units of 100H. Addresses for which'0H' is set are not protected .

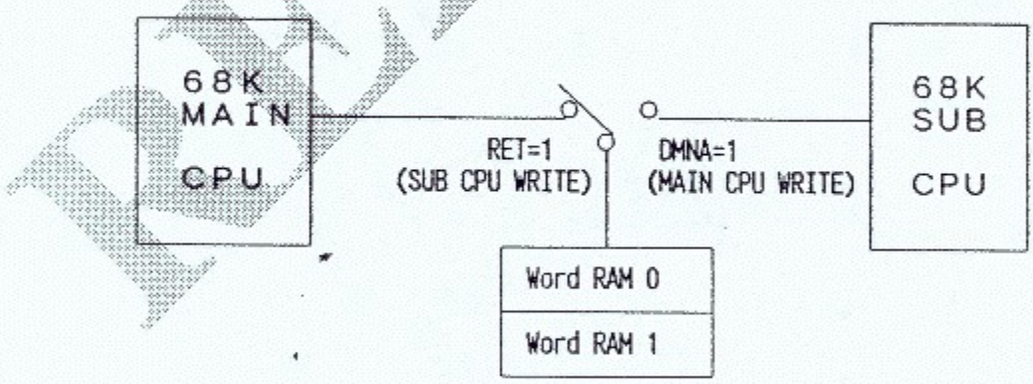
●Word RAM switching in the 1M mode



DMNA bit in this mode : Only the main CPU is able to write to this bit. Only '1' is significant, indicating a switchover request. '0' is set by hardware.
When this bit is read, '1' indicates that switching is in progress and '0' that switching is finished.

RET bit in this mode : Only the SUB-CPU is able to write to this bit. '1' indicates that WORD-RAM1 is assigned to the MAIN-CPU and WORD-RAM0 ti the SUB-CPU. '0' indicates that WORD-RAM0 is assigned to the MAIN-CPU and WORD-RAM1 to the SUB-CPU.
When this bit is read, its value is either '0' or '1' when switching is finished.

●Word RAM switching in the 2M mode



DMNA bit in this mode : Only the main CPU is able to write to this bit. Only '1' is significant, indicating that WORD-RAM0 and WORD-RAM1 are assigned to the SUB-CPU.

RET bit in this mode : Only the SUB-CPU is able to write to this bit. Only '1' is significant, indicating that WORD-RAM0 and WORD-RAM1 are assigned to the MAIN-CPU.

If DMNA=0 and RET=0 (immediately after power-on only), the atatus is neutral. Then the hardware switches the status to DMNA=0 and RET=1 (word RAM assigned to the MAIN-CPU). If DMNA is then set to '1', the status becomes DMNA=1, RES=1. This is also a neutral status, and the hardware then switches the status to DMNA=1 and RET=0 (word RAM assigned to the SUB-CPU). In order words, 0, 0 status occurs only right after power-on or after switching from the 1M to the 2M mode. Also, neutral status is always followed by a single refresh.

6. CDC

●$OFF8004 :CDC mode / CDC RS0

MSB LSB

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
	EDT	DSR	—	—	—	DD2	DD1	DD0	—	—	—	—	CA3	CA2	CA1	CA0
RD	0/1	0/1	0	0	0	0/1	0/1	0/1	0	0	0	0	0/1	0/1	0/1	0/1
WR	0	0	0	0	0	0/1	0/1	0/1	0	0	0	0	0/1	0/1	0/1	0/1

CA0-3 : CDC register address
Refer to the LC89510 (Sanyo) manual for information on how to use this register.
DSR : Data set ready
Indicates that data from the CDC has been set in the $0FF8008 register.
EDT : End of data transfer
All data from the CDC has been transferred.
DD0-2 : Device destination

			Destination	
DD2	DD1	DD0	2M MODE	1M MODE
0	0	0	Setting not allowed	Setting not allowed
0	0	1	Setting not allowed	Setting not allowed
0	1	0	MAIN CPU READ	MAIN CPU READ
0	1	1	SUB CPU READ	SUB CPU READ
1	0	0	RF5C164(PCM) DMA	RF5C164(PCM) DMA
1	0	1	PRG.-RAM DMA	PRG.-RAM DMA
1	1	0	Setting not allowed	Setting not allowed
1	1	1	2M RAM DMA	SUB CPU 1M RAM DMA

●$OFF8006 : CDC RS1

MSB LSB

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0
RD	0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
WR	0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

● CD0~7 : CDC register data
Refer to the LC89510 (Sanyo) manual for information on how to use this register.

●$OFF8008 : CDC host data (16bit)

MSB LSB

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
	HD15	HD14	HD13	HD12	HD11	HD10	HD09	HD08	HD07	HD06	HD05	HD04	HD03	HD02	HD01	HD00
RD	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
WR	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

HD00-15 : CDC read data bits 00-15.
After two bytes of the (8bit) data from the CDC is stored, it is transferred to the MAIN-CPU and SUB-CPU. If this data is not read immediately, the CDC waits until it is.

●$OFF800A : CDC DMA address

MSB LSB

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
	A18	A17	A16	A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03
RD	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
WR	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

In the case of RF5C164 (PCM), the bits up to A12 are used and A13-A17 are '0'. If the memory is divided into MAIN RAM (1M) and SUB-RAM (1M), the bits up to A16 are used, and A17 and A18 are '0'. In the 2M-RAM mode A18 is '0'. For PROG.-RAM, all bits are used.

●$OFF800C : Stopwatch

MSB LSB

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	SW11	SW10	SW09	SW08	SW07	SW06	SW05	SW04	SW3	SW02	SW01	SW00
RD	O	O	O	O	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
WR	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO

SW00-11 : Timer data bits 00-11
This is a general use timer, but it is mainly used for CDC and CDD measurement.
Each clock tick represents 30.72μs and the counter range is 0-4095.
Writeing (0 only) to the counter clears it.
WO : 0 only (data write).

7. COMMUNICATION

●$OFF800E : Communication flag

MSB LSB

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
	CFM7	CFM6	CFM5	CFM4	CFM3	CFM2	CFM1	CFM0	CFS7	CFS6	CFS5	CFS4	CFS3	CFS2	CFS1	CFS0
RD	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
WR	O	O	O	O	O	O	O	O	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

CFS0-7 : SUB-CPU communication flag bits 0-7 .
Flag for communication from SUB-CPU to main CPU.
CFM0-7 : Main CPU communication flag bits 0-7.
Flag for communication from MAIN-CPU to SUB-CPU.

●$OFF8010~$OFF801E

Communication command, 8 words, read only.

●$OFF8020~$OFF802E

Communication status, 8 words, ~~read only~~. Read/write

8. GENERAL USE TIMER

●$OFF8030 : Timer W/INT3

MSB LSB

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	TD7	TD6	TD5	TD4	TD3	TD2	TD1	TD0
RD	0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
WR	0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

TD0-7 : Timer data bits 0-7.
Each clock tick represents 30.72 μs and, if a value has been written for n, the counter counts down from n-0 repeatedly ($0 < n \leq 255$). When the counter reaches 0 INT LEVEL3 is issued. If n is set to 0 INT3 is not issued.
When these bits are read the set value is returned.

9. INTTERUPTS

●$OFF8032 : Interrupt mask control

MSB LSB

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	–
RD	0	0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0
WR	0	0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0

IEN1-6 : Interrupt enable level 1-6.
Used to enable or disable the various interrupts.
'0'=enable, '1'=disable.
The mask status can be determined by reading these bits.

Level 6 : Subcode (98-byte buffering finished)
Level 5 : CDC (error correction)
Level 4 : CDD (reception of receive status 7 completed)
Level 3 : Timer (down counter has reached 0)
Level 2 : MD (V-INT by software command, etc.)
Level 1 : Graphic complete (only in 2M mode)

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10. CDD

●$OFF8034 : CD fader

MSB LSB

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
	EFDT	FD10	FD09	FD08	FD07	FD06	FD05	FD04	FD03	FD02	FD01	FD00	DEF1	DEF0	SSF	—
RD	0/1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
WR	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0

FD00-10 : Fade volume data bits 00-11
Soft mute is performed when $4000 changes to $0000 (off at 23.2ms).
Spindle speed flag.

SSF : Spindle speed flag
'0'=normal speed playback, '1' twice normal speed playback.

EFDT : End of fade data transfer.
Reports when transfer of the set data is complete.
'0'=end, '1' transfer in progress.

DEF 1,0 : De-emphasis flag

DEF1	DEF0	OPERATION
0	0	OFF
0	1	Fs=44.1KHz
1	0	Fs=32KHz
1	1	Fs=48KHz

Normally off

Some old classical CDs contain emphasis data.

●$OFF8036 : CDD control

MSB LSB

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	D/M	—	—	—	—	—	HOCK	DRS	DTS
RD	0	0	0	0	0	0	0	0/1	0	0	0	0	0	0/1	0/1	0/1
WR	0	0	0	0	0	0	0	0	0	0	0	0	0	0/1	WO	WO

WO: '0' only during line status.

DTS : Data transfer status.
'1' when signals are being transferred from the communication buffer to the CDD (communication is suspended for 240μs if a communication error is generated). Writing a '0' forces termination.

DRS : Data receive status
'1' when signals are being transferred from the CDD to the communication buffer (communication is suspended for 240μs if a communication error is generated). Writing a '0' forces termination.

HOCK : Host clock
'0' at power-on. Setting this bit to one causes communication with the CDD to commence.

D/M : Data/muting
Indicates whether the data being output from the CDD is ROM data or music data.
'1'=data (Includes STOP and PAUSE status in addition to when music data is being output.)
'0'=misic

●$OFF8038~OFF804A : Communication with CDD

MSB LSB

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0				Receive status 0				0				Receive status 1			
0				Receive status 2				0				Receive status 3			
0				Receive status 4				0				Receive status 5			
0				Receive status 6				0				Receive status 7			
0				Receive status 8				0				Receive status 9			
0				Transfer command 0				0				Transfer command 1			
0				Transfer command 2				0				Transfer command 3			
0				Transfer command 4				0				Transfer command 5			
0				Transfer command 6				0				Transfer command 7			
0				Transfer command 8				0				Transfer command 9			

When receiving is finished in receive status 7 INT4 is issued. Data transfer to the CDD begins when transfer command 9 is written by the SUB-CPU.

11. COLOR CALCULATION

●$OFF804C : Font color

MSB LSB

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	SC13	SC12	SC11	SC10	SC03	SC02	SC01	SC00
RD	0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
WR	0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

SC00-03 : Source color data 00-03
Color data assigned to places for which $12 data is set to '0'.

SC10-13 : Source color data 10-13
Color data assigned to places for which $12 data is set to '1'.

●$OFF804E : Font bit

MSB LSB

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
	SBF	SBE	SBD	SBC	SBB	SBA	SB9	SB8	SB7	SB6	SB5	SB4	SB3	SB2	SB1	SB0
RD	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
WR	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

SFB0-F : Source font bits 0-f
This is the register to which the raw data for kanji fonts, etc. is input.
The source color data above this data is selected and converted to the MEGA DRIVE video format. The conversion data is contained in the following register.

●$OFF8050~$OFF8056 : Font data (Read only)

MSB LSB

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
FDF3	FDF2	FDF1	FDF0	FDE3	FDE2	FDE1	FDE0	FDD3	FDD2	FDD1	FDD0	FDC3	FDC2	FDC1	FDC0
FDB3	FDB2	FDB1	FDB0	FDA3	FDA2	FDA1	FDA0	FD93	FD92	FD91	FD90	FD83	FD82	FD81	FD80
FD73	FD72	FD71	FD70	FD63	FE62	FD61	FD60	FD53	FD52	FD51	FD50	FD43	FD42	FD41	FD40
FD33	FD32	FD31	FD30	FD23	FD22	FD21	FD20	FD13	FD12	FD11	FD10	FD03	FD02	FD01	FD00

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12. ROTATION COMPRESSION

●$OFF8058 : Stamp size

MSB LSB

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	–	–	–	–	–	SMS	STS	RPT
RD	0	0	0	0	0	0	0	0	0	0	0	0	0	0/1	0/1	0/1
WR	0	0	0	0	0	0	0	0	0	0	0	0	0	0/1	0/1	0/1

STS : Stamp size
Specifies the size of the stamps which comprise the stamp map.
'0'=16x16 dots
'1'=32x32 dots

SMS : Stamp map size
'0'=1x1 screen (256x256 dots)
'1'=16x16 screens (4,098x4,098 dots)

RPT : Repeat
'0'=The map is repeated when the stamp map size is reached.
'1'=Data which exceeds the stamp map size is set to '0'.

●$OFF805A : Stamp map base address

If SMS=0,STS=0 (1x1 screen, 16x16 dots) 200H

MSB LSB

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
	A17	A16	A15	A14	A13	A12	A11	A10	A09	–	–	–	–	–	–	–
RD	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0	0	0	0	0	0	0
WR	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0	0	0	0	0	0	0

If SMS=0,STS=1 (1x1 screen, 32x32 dots)

MSB LSB

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
	A17	A16	A15	A14	A13	A12	A11	A10	A09	A08	A07	–	–	–	–	–
RD	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0	0	0	0	0
WR	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0	0	0	0	0

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If SMS=1,STS=0 (16x16 screens, 16x16 dots)
In this case A17 is fixed at '1'.

If SMS=1,STS=1 (16x16 screens, 32x32 dots)

MSB LSB

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
	A17	A16	A15	—	—	—	—	—	—	—	—	—	—	—	—	—
RD	0/1	0/1	0/1	0	0	0	0	0	0	0	0	0	0	0	0	0
WR	0/1	0/1	0/1	0	0	0	0	0	0	0	0	0	0	0	0	0

These addresses determine where the map is to be allocated when MAIN-RAM is in the 2M mode.

The stamp data is as follows.

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
HFLP	RT1	RT0	0	0	SN0A	SN09	SN08	SN07	SN06	SN05	SN04	SN03	SN02	SN01	SN00

HELP : Left-right rotation
SN00-A : The stamp No. With 32x32 dot stamps, SN00 and SN01 should be set to 0.
RT1,0 : 0° , 90° , 180° , 270°

The address area of the charater generator is allocated as the top of 2M RAM ($080000 if assigned to the SUB-CPU.) The character generator sequence is the same as that of the MEGA DRIVE sprite.

The address sequence for 16x16 dot stamps is as follows.

$00	$01	$02	$03	$40	$41	$42	$43
$04	$05	$06	$07	$44	$45	$46	$47
$08	$09	$0A	$0B	$48	$49	$4A	$4B
$0C	$0D	$0E	$0F	$4C	$4D	$4E	$4F
$10	$11	$12	$13	$50	$51	$52	$53
$14	$15	$16	$17	$54	$55	$56	$57
$18	$19	$1A	$1B	$58	$59	$5A	$5B
$1C	$1D	$1E	$1F	$5C	$5D	$5E	$5F
$20	$21	$22	$23	$60	$61	$62	$63
$24	$25	$26	$27	$64	$65	$66	$67
$28	$29	$2A	$2B	$68	$69	$6A	$6B
$2C	$2D	$2E	$2F	$6C	$6D	$6E	$6F
$30	$31	$32	$33	$70	$71	$72	$73
$34	$35	$36	$37	$74	$75	$76	$77
$38	$39	$3A	$3B	$78	$79	$7A	$7B
$3C	$3D	$3E	$3F	$7C	$7D	$7E	$7F

1 dot for D7-D4 and 1 dot for D3-D0.

The top left corner is D7-D4 of $00.

The bottom right corner is D3-D0 of $7F.

The address sequence for 32x32 dot stamps is as follows.

$000 $001 $002 $003 $080 $081 $082 $083 $100 $101 $102 $103 $180 $181 $182 $183
$004 $005 $006 $007 $084 $085 $086 $087 $104 $105 $106 $107 $184 $185 $186 $187
$008 $009 $00A $00B $088 $089 $08A $08B $108 $109 $10A $10B $188 $189 $18A $18B
$00C $00D $00E $00F $08C $08D $08E $08F $10C $10D $10E $10F $18C $18D $18E $18F
$010 $011 $012 $013 $090 $091 $092 $093 $110 $111 $112 $113 $190 $191 $192 $193
$014 $015 $016 $017 $094 $095 $096 $097 $114 $115 $116 $117 $194 $195 $196 $197
$018 $019 $01A $01B $098 $099 $09A $09B $118 $119 $11A $11B $198 $199 $19A $19B
$01C $01D $01E $01F $09C $09D $09E $09F $11C $11D $11E $11F $19C $19D $19E $19F
$020 $021 $022 $023 $0A0 $0A1 $0A2 $0A3 $120 $121 $122 $123 $1A0 $1A1 $1A2 $1A3
$024 $025 $026 $027 $0A4 $0A5 $0A6 $0A7 $124 $125 $126 $127 $1A4 $1A5 $1A6 $1A7
$028 $029 $02A $02B $0A8 $0A9 $0AA $0AB $128 $129 $12A $12B $1A8 $1A9 $1AA $1AB
$02C $02D $02E $02F $0AC $0AD $0AE $0AF $12C $12D $12E $12F $1AC $1AD $1AE $1AF
$030 $031 $032 $033 $0B0 $0B1 $0B2 $0B3 $130 $131 $132 $133 $1B0 $1B1 $1B2 $1B3
$034 $035 $036 $037 $0B4 $0B5 $0B6 $0B7 $134 $135 $136 $137 $1B4 $1B5 $1B6 $1B7
$038 $039 $03A $03B $0B8 $0B9 $0BA $0BB $138 $139 $13A $13B $1B8 $1B9 $1BA $1BB
$03C $03D $03E $03F $0BC $0BD $0BE $0BF $13C $13D $13E $13F $1BC $1BD $1BE $1BF
$040 $041 $042 $043 $0C0 $0C1 $0C2 $0C3 $140 $141 $142 $143 $1C0 $1C1 $1C2 $1C3
$044 $045 $046 $047 $0C4 $0C5 $0C6 $0C7 $144 $145 $146 $147 $1C4 $1C5 $1C6 $1C7
$048 $049 $04A $04B $0C8 $0C9 $0CA $0CB $148 $149 $14A $14B $1C8 $1C9 $1CA $1CB
$04C $04D $04E $04F $0CC $0CD $0CE $0CF $14C $14D $14E $14F $1CC $1CD $1CE $1CF
$050 $051 $052 $053 $0D0 $0D1 $0D2 $0D3 $150 $151 $152 $153 $1D0 $1D1 $1D2 $1D3
$054 $055 $056 $057 $0D4 $0D5 $0D6 $0D7 $154 $155 $156 $157 $1D4 $1D5 $1D6 $1D7
$058 $059 $05A $05B $0D8 $0D9 $0DA $0DB $158 $159 $15A $15B $1D8 $1D9 $1DA $1DB
$05C $05D $05E $05F $0DC $0DD $0DE $0DF $15C $15D $15E $15F $1DC $1DD $1DE $1DF
$060 $061 $062 $063 $0E0 $0E1 $0E2 $0E3 $160 $161 $162 $163 $1E0 $1E1 $1E2 $1E3
$064 $065 $066 $067 $0E4 $0E5 $0E6 $0E7 $164 $165 $166 $167 $1E4 $1E5 $1E6 $1E7
$068 $069 $06A $06B $0E8 $0E9 $0EA $0EB $168 $169 $16A $16B $1E8 $1E9 $1EA $1EB
$06C $06D $06E $06F $0EC $0ED $0EE $0EF $16C $16D $16E $16F $1EC $1ED $1EE $1EF
$070 $071 $072 $073 $0F0 $0F1 $0F2 $0F3 $170 $171 $172 $173 $1F0 $1F1 $1F2 $1F3
$074 $075 $076 $077 $0F4 $0F5 $0F6 $0F7 $174 $175 $176 $177 $1F4 $1F5 $1F6 $1F7
$078 $079 $07A $07B $0F8 $0F9 $0FA $0FB $178 $179 $17A $17B $1F8 $1F9 $1FA $1FB
$07C $07D $07E $07F $0FC $0FD $0FE $0FF $17C $17D $17E $17F $1FC $1FD $1FE $1FF

1 dot for D7-D4 and 1 dot for D3-D0.
The top left corner is D7-D4 of $00.
The bottom right corner is D3-D0 of $1FF.

The sequence of stamps in the stamp map is horizontal (Same MD)
The stamp size can be either 16x16 or 32x32 dots.
The stamp map size can be either 1x1 or 16x16 screens.

```
S0   S1   S2   S3   . . . . . .
Sn   Sn+1 Sn+2 Sn+3 . . . . . .
.    .    .    .    . . . . . .
.    .    .    .    . . . . . .
```

●$OFF805C : Image buffer V cell size (0-32 cells) Minus One

MSB LSB

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	VCS4	VCS3	VCS2	VCS1	VCS0
RD	0	0	0	0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1
WR	0	0	0	0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1

VCS0-4 : Specifies the number of vertical cells in the image buffer.

●$OFF805E : Image buffer start address

MSB LSB

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
	A17	A16	A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	—	—	—
RD	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0	0	0
WR	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0	0	0

●$OFF8060 : Image buffer offset

MSB LSB

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	LN2	LN1	LN0	dot2	dot1	dot0
RD	0	0	0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1
WR	0	0	0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1

LN0-2 : Indicates the number of lines in the start cell written to the image buffer.
DOT0-2 : Indicates the number of dots corresponding to the above number of lines.

●$OFF8062 : Image buffer H dot size (horizontal dot size overwritten in the buffer)

MSB LSB

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	HW08	HW07	HW06	HW05	HW04	HW03	HW02	HW01	HW00
RD	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
WR	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

HW00-08 :Determines the number of dots which can be written horizontally in the place determined by the image buffer start address and image buffer offset.

●$OFF8064 : Image buffer V dot size (vertical dot size overwritten in the buffer)

MSB LSB

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	VW07	VW06	VW05	VW04	VW03	VW02	VW01	VW00
RD	0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
WR	0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

VW00-08 : Determines the number of dots which can be written vertically in the place determined by the image buffer start address and image buffer offset.

●$OFF8066 : Trace vector base address(Xstart, Ystart,(Delta)X,(Delta)Y table base address)

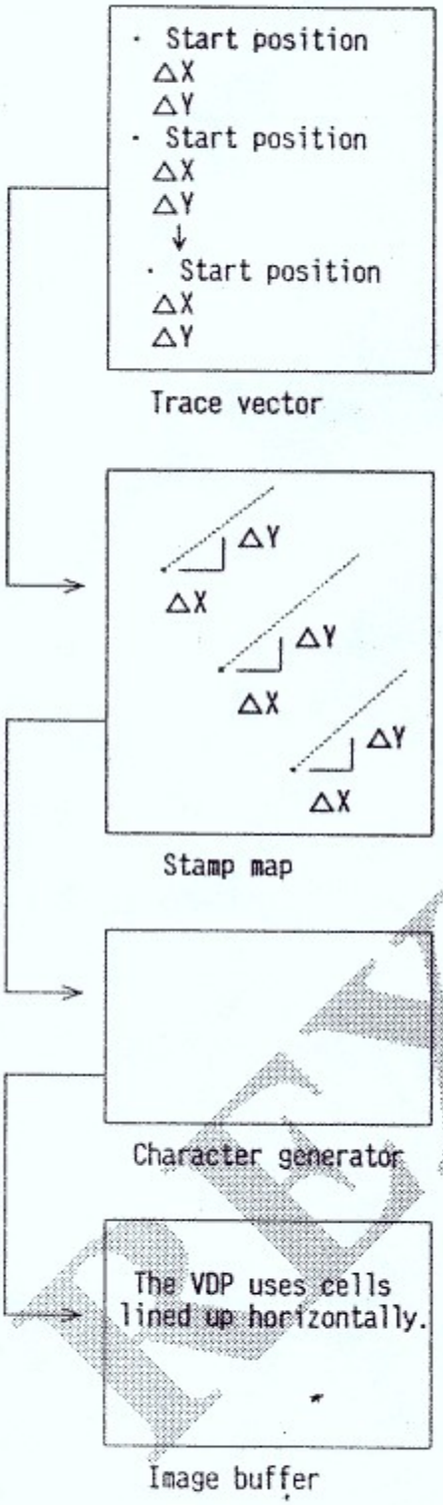
MSB LSB

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
	A17	A16	A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	—
RD	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0
WR	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0

Coordinate conversion begins when this is set.

Start position,dX,dY → Stamp map → Character generator → Image buffer table

REX



← Coordinate conversion begins when this trace vector base address is set.

○These start positions, △X and △Y coordinates are calculated by the SUB-CPU. (These three make up one line.)

○The number of lines converted depends on the V dot size ($0FF8064).

○The place to which △X and △Y coordinates are calculated from the startposition is sampled vased on the H dot size ($0FF8062).

○A character apperars in the place where sampling took place in the stamp map stage.

○The characters are stored in the MD V-RAM.

○When the final dot is written, interrupt level one is issued.

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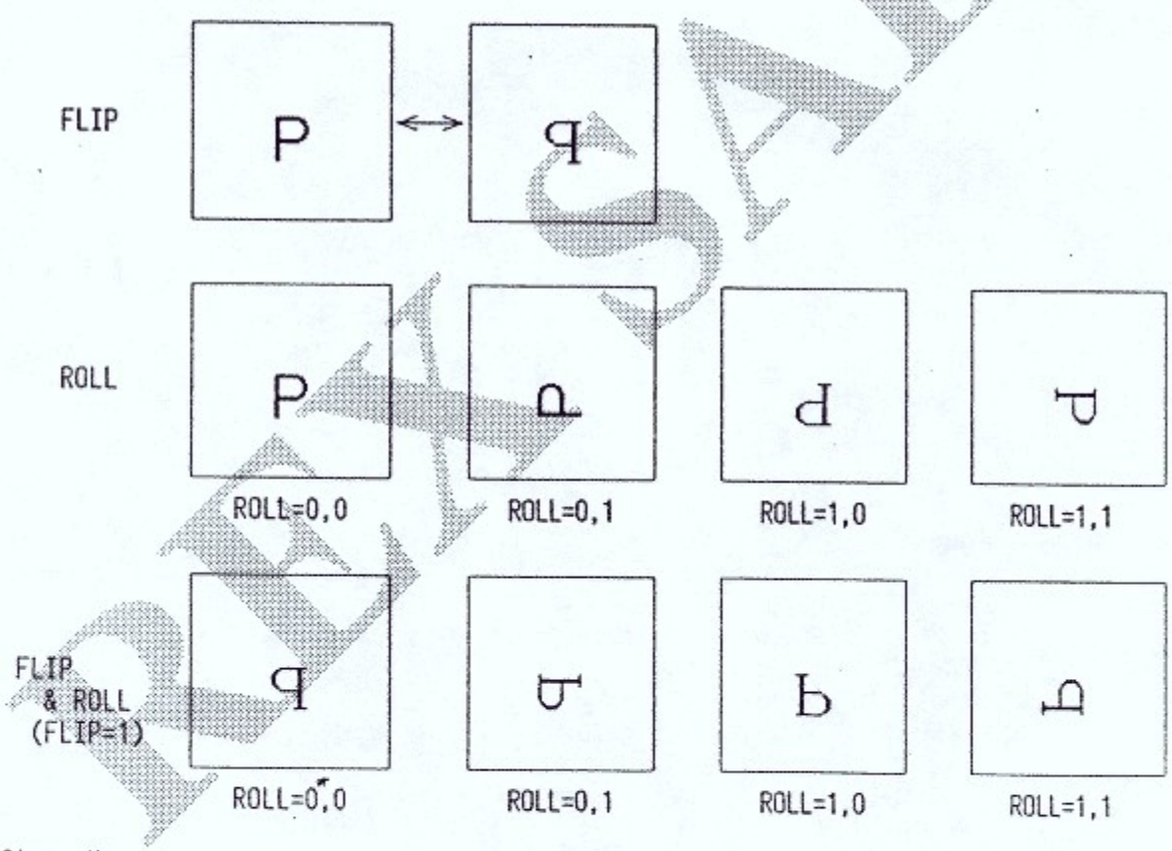
●Stamp structure

· 16x16 dot stamps

FLIP	ROLL	Stamp No.												
	1 , 0	O	O	SNO A	SNO 9	SNO 8	SNO 7	SNO 6	SNO 5	SNO 4	SNO 3	SNO 2	SNO 1	SNO 0

· 32x32 dot stamps

FLIP	ROLL	Stamp No.												
	1 , 0	O	O	SNO A	SNO 9	SNO 8	SNO 7	SNO 6	SNO 5	SNO 4	SNO 3	SNO 2	O	O



○Stamp No.

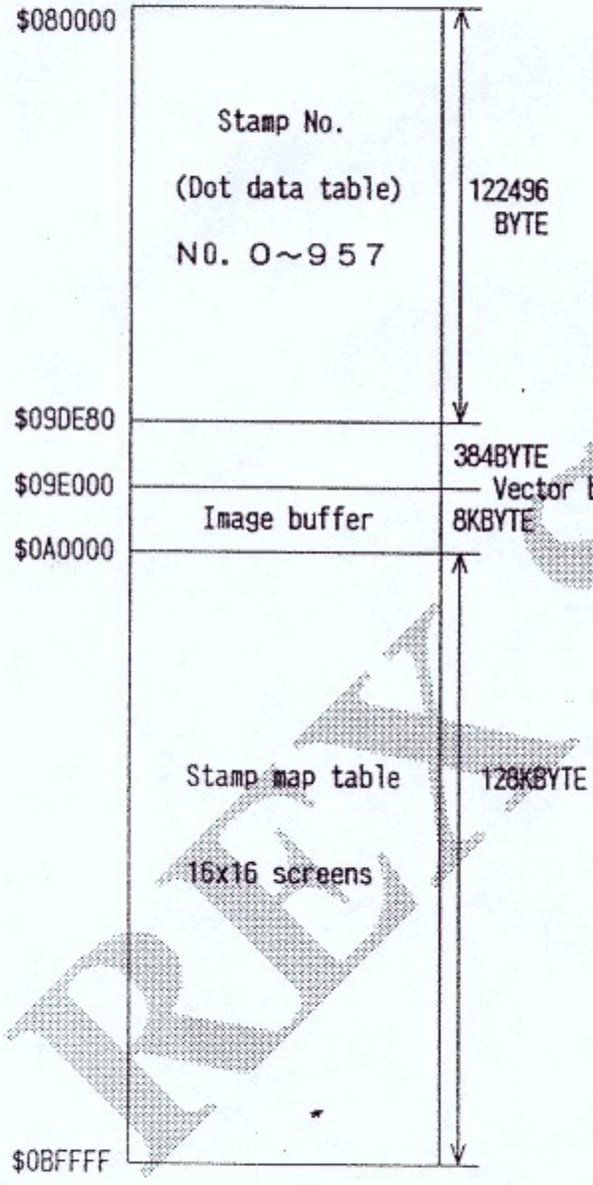
· 16x16 dot : Up to 2,048 can be specified in SNO A-0.
· 32x32 dot : Up to 512 can be specified in SNO A-2.

SEGA

●Rotation mode mapping example

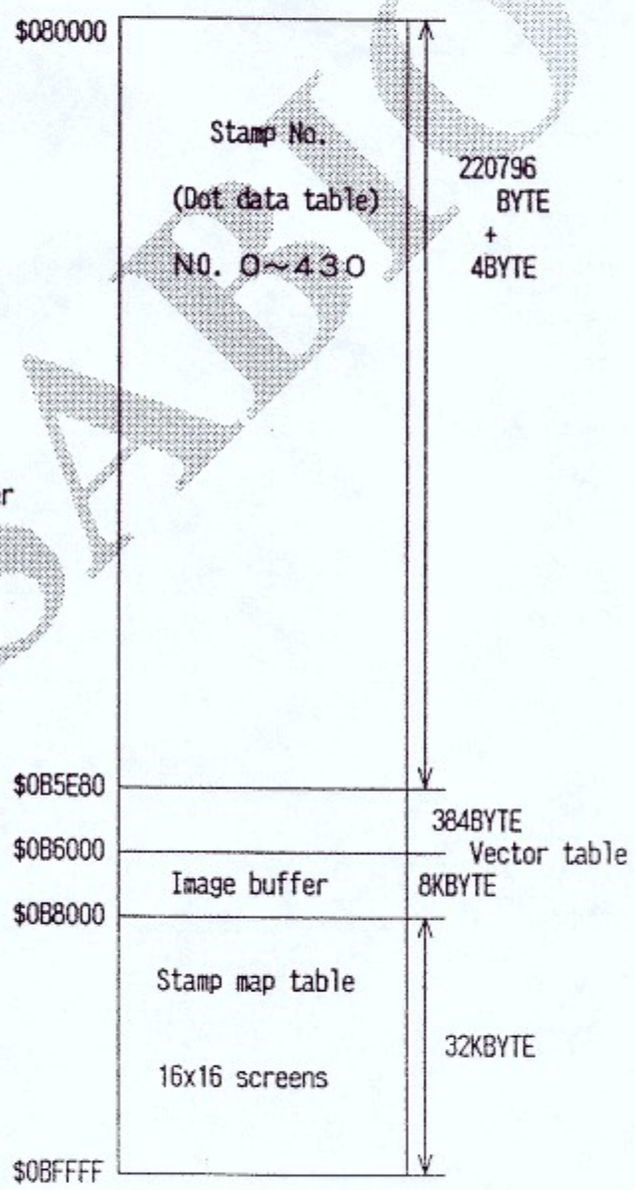
16×16 dot stamps
16×16 screen mode
Image buffer(6x38 cells)
Vector table (6x8 lines)

Assigned to SUB-CPU



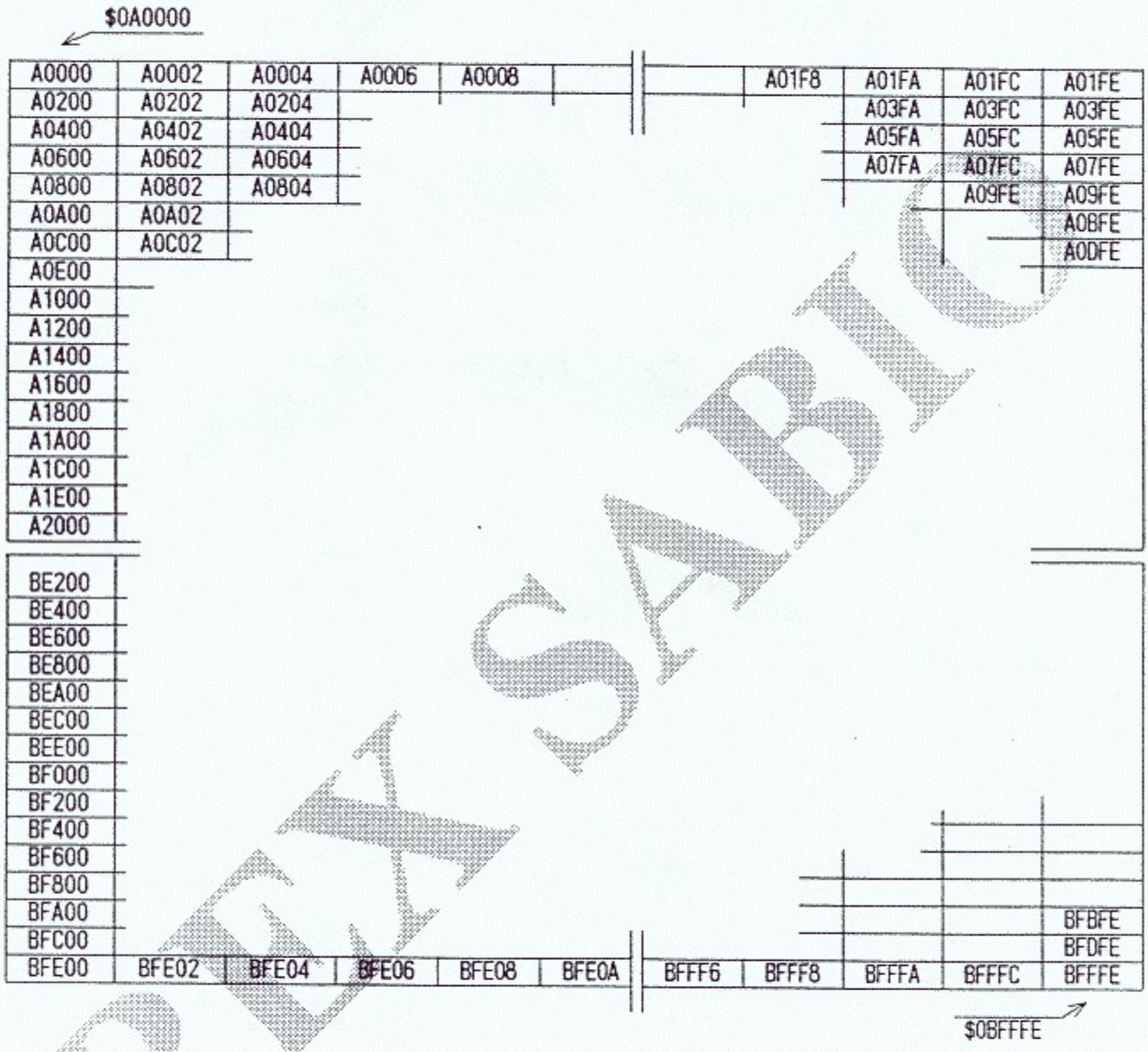
32×32 dot stamps
16×16 screen mode
Image buffer(6x38 cells)
Vector table(6x8 lines)

Assigned to SUB-CPU



RELEASED

●Stamp map base address area with 16x16 screens and 16x16 dot stamps



REX SABIC

●Stamp map base address area with 16x16 screens and 32x32 dot stamps

Base address

000	002	004	006	008			0F8	0FA	0FC	0FE
100	102	104						1FA	1FC	1FE
200	202	204						2FA	2FC	2FE
300	302	304						3FA	3FC	3FE
400	402	404							4FE	4FE
500	502									5FE
600	602									6FE
700										
800										
900										
A00										
B00										
C00										
D00										
E00										
F00										
1000										
7100										
7200										
7300										
7400										
7500										
7600										
7700										
7800										
7900										
7A00										
7B00									7AFC	7AFE
7C00									7BFC	7BFE
7D00								7CFC	7CFC	7CFE
7E00								7DFA	7DFC	7DFE
7F00	7F02	7F04	7F06	7F08	7F0A	7FF6	7FF8	7EFA	7EFE	7EFE
								7FFA	7FFC	7FFE

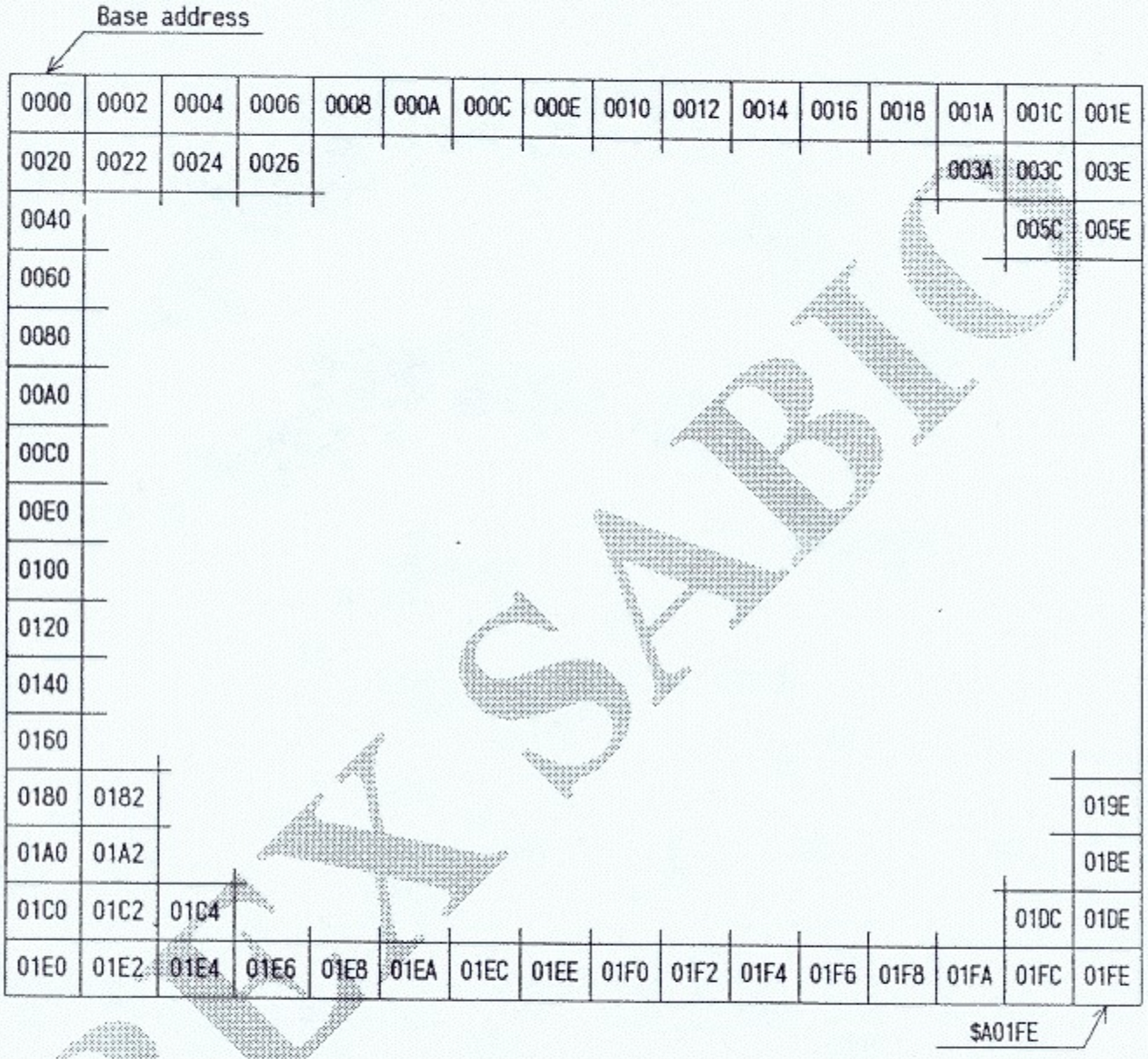
○Stamp map base address

$080000
$088000
$090000
$098000
$0A0000
$0A8000
$0B0000
$0B8000

The left eight banks are availlable for use.
In practice, an area in which todefine the stamp data is neccessary, so some of the eight banks will be unusable.

SEGA SABIC

●Stamp map base address area with 1x1 screen and 16x16 dot stamps.



○Stamp map base address

$080000
$080200
$080400
$080600
$080800
Up to 512 banks in 200H units can be used.
$0BFC00
$0BFE00

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●Stamp map base address area with 1x1 screen and 32x32 dot stamps.

0000	0002	0004	0006	0008	000A	000C	000E
0010	0012	0014	0016	0018	001A	001C	001E
0020	0022	0024	0026	0028	002A	002C	002E
0030							003E
0040							004E
0050							005E
0060							006E
0070	0072	0074	0076	0078	007A	007C	007E

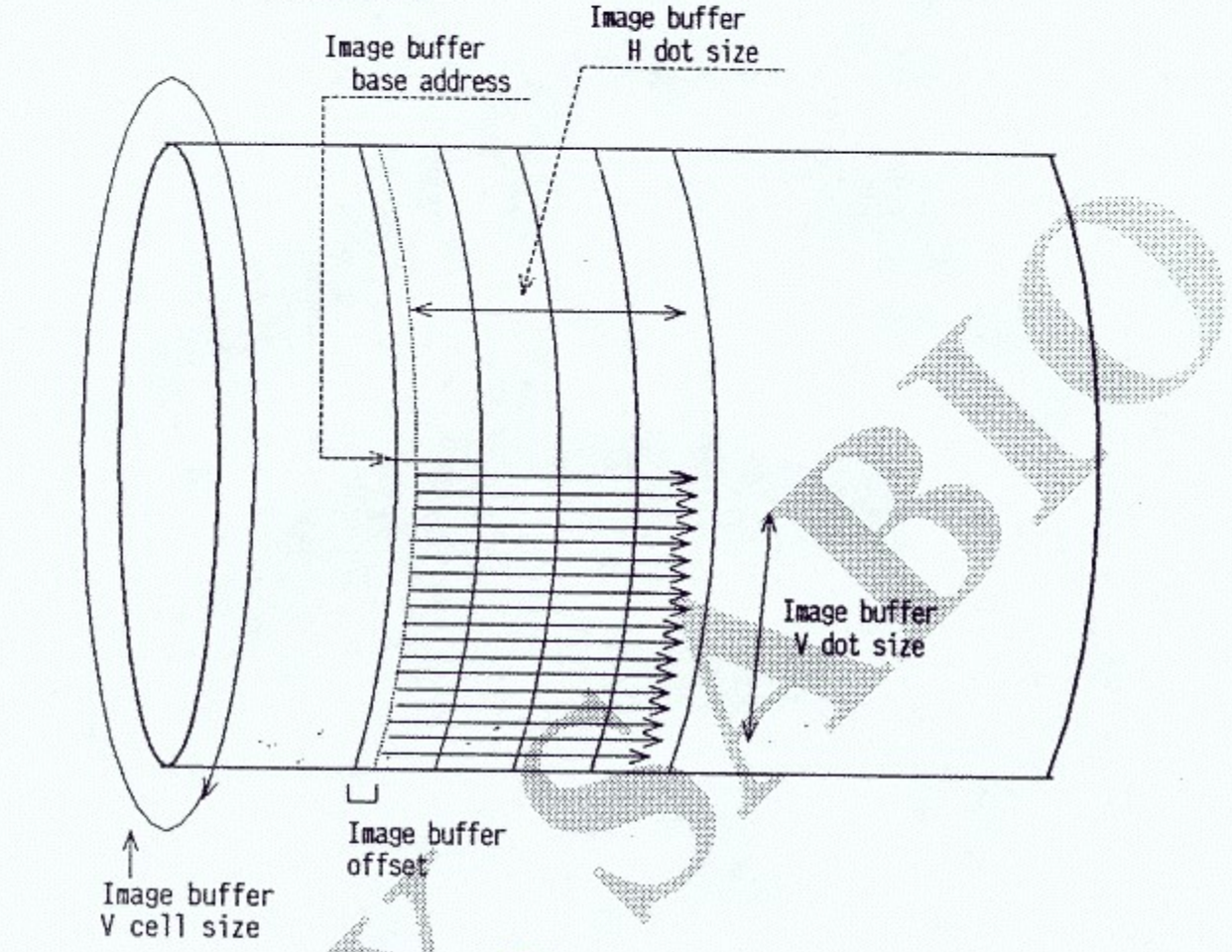
○Stamp map base address

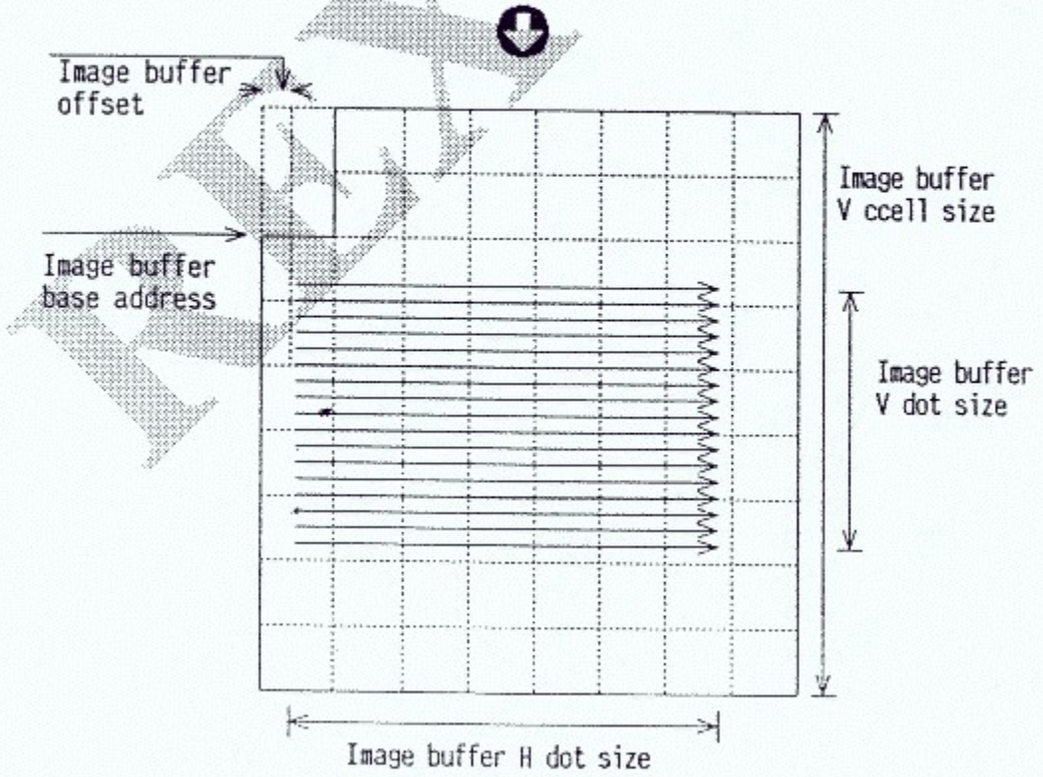
$080000
$080080
$080100
$080180
$080200
:
$0BFF00
$0BFF80

} Up to 2,048 banks in 80H units can be used.

REA SAED

●Basic overview of image buffer





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13. SUBCODES

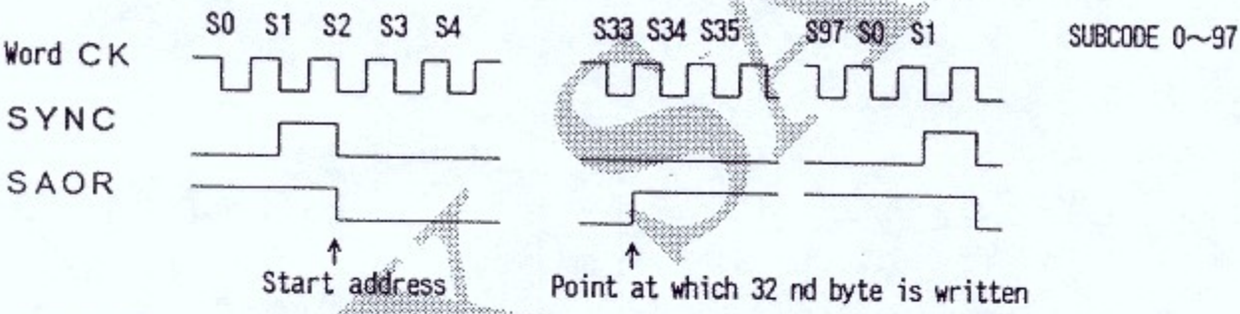
●$0FF8068 : Subcode address

MSB LSB

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	SAOR	STA6	STA5	STA4	STA3	STA2	STA1	–
RD	0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0
WR	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–

STA1-6 : Subcode top address.
After previous data has been input,this is the address at which new data will be input.

SAOR : Subcode address overrun
'1' when 32 bytes have been written.
Cleared by SYNC.



●$0FF806A~$0FF80FE

Reserved by SEGA

●$0FF8100~$0FF817E

64-wordx16-bit subcode buffer area.

●$0FF8180~$0FF81FE

Imageofsubcodebufferarea.

SEGA

14. MAIN-CPU

●$0A12000 : RESET,HALT

MSB LSB

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	IFL2	–	–	–	–	–	–	SBRQ	SRES
RD	0	0	0	0	0	0	0	0/1	0	0	0	0	0	0	0/1	0/1
WR	0	0	0	0	0	0	0	0/1	0	0	0	0	0	0	0/1	0/1

SRES : SUB-CPU reset
'0'=Reset / '1'=Run

SBRQ : SUB-CPU bus request.
Write: '0'= Cancel / '1' Request.
Read : '0'=SUB-CPU operating / '1' =acknowledge.

IFL2 : Send interrupt level 2 to SUB-CPU.
'1'=Intterrupt / '0'=Ackowledge returned.

●$0A12002 : Memory mode / Write protect

MSB LSB

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
	WP7	WP6	WP5	WP4	WP3	WP2	WP1	WP0	BK1	BK0	–	–	–	MODE	DMNA	RET
RD	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0	0	0	0/1	0/1	0/1
WR	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0	0	0	0	0/1	0

WP0-7 : By writeing addresses to these bits SUB-CPU area $0-$0FEFF can be write protected in 100H increments. No write protect when set to '0'.

MODE : RAM mode
'0' = 2Mbit '1'=1Mbit

DMNA : Declaration of MAIN-CPU no access on RAM.
Mode='0'(2M mode): See the SUB-CPU description for details.
If the declaration bit which indicates that the MAIN-CPU cannot access the 2M MAIN-RAM area is set to '1', the entire 2M RAM area is assigned to the SUB-CPU.
If it is set to '0', the 2M RAM area is assiigned to the MAIN-CPU.
Mode='1' (1M mode): A swap request is sent to the SUB-CPU by setting this bit to '1'.
'0' indicates swap compllleted.

BK0,1 : When the PROG.-RAM (4Mbit) is accessed by the MAIN-CPU, only a 1Mbit area can be assigned to the MAIN-CPU at any one time. It is therefore divided into four banks to facilitate access.

PROTOTYPE

RET : RET bit
Mode = '0' (2M mode) : See the SUB-CPU description for detaills.
In contrast to DMNA, this is the bit reaturns the 2M RAM area to the MAIN-CPU.
When set to '1' the 2M RAM area is assigned to the MAIN-CPU.
When set to '0' it is assigned to the SUB-CPU.
Mode='1' : '0'=WORD-RAM0(1M) is assigned to the MAIN-CPU and WORD RAM1(1M) assigned to the SUB-CPU.
'1'=WORD-RAM1(1M) is assigned to the MAIN-CPU and WORD-RAM0 (1M) assigned to the SUB-CPU.

15. CDC

●$0A12004 : CDC mode

MSB LSB

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
	EDT	DSR	—	—	—	DD2	DD1	DD0	—	—	—	—	—	—	—	—
RD	0/1	0/1	0	0	0	0/1	0/1	0/1	0	0	0	0	0	0	0	0
WR	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

DD0-2 : Device destination
See the description ofSUB-CPU register $0FF8004.
EDT : Send sub data transfer.
Indicates that all of the data from the CDC has been transferred.
DSR : DATA set ready.
Indicates that data has been set in the $0A12008 register by the CDC.

●$0A12006 : H-INT vector

MSB LSB

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
	HI8F	HI8E	HI8D	HI8C	HI8B	HI8A	HI89	HI88	HI87	HI86	HI85	HI84	HI83	HI82	HI81	HI80
RD	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
WR	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

When H-INT is issued from the MAIN-CPU, $70=00FFH(ROM data) and $72=the above 16 bits.
This becomes the jump target. It is set to -1 immediatelly after reset.

●$0A12008 CDC : CDC host data (16bit)

MSB LSB

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
	HD15	HD14	HD13	HD12	HD11	HD10	HD09	HD08	HD07	HD06	HD05	HD04	HD03	HD02	HD01	HD00
RD	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
WR	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

●$0A1200A
Resetved by SEGA

●$0A1200C : Stopwatch

MSB LSB

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	TD11	TD10	TD09	TD08	TD07	TD06	TD05	TD04	TD03	TD02	TD01	TD00
RD	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
WR	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

TD00-11 : Timer data
Each clock tick represents 30.72μs and the counter range is 0-4095.
The timer is set using SUB-CPU $0FF800C.

16. COMMUNICATION

●$0A1200E : Communication flag

MSB LSB

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
	CFM7	CFM6	CFM5	CFM4	CFM3	CFM2	CFM1	CFM0	CFS7	CFS6	CFS5	CFS4	CFS3	CFS2	CFS1	CFS0
RD	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
WR	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	—	—	—	—	—	—	—	—

CFM0-7 : Main-CPU communication flag.
CFS0-7 : SUB—CPU communication flag.

●$0A12010~$0A1201E : Communication command.
8—Word, read/write.

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●$0A12020~$0A1202E : Communication Status.
8-Word, read only.

---- MEGA-CD MANUAL END ----

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