T-77-13

RICOH

EK-013-8811

# PCM Sound Generator IC

# RF5C68A

## ■ GENERAL DESCRIPTION

RF5C68A is a sound generator IC that uses pulse code modulation (PCM). It has a digital control oscillator (DCO) and digital control amplifier (DCA) built in. You can structure a PCM sound generator system by connecting external waveform data memories (pseudo SRAM, SRAM, or mask ROM) and D/A converters, controlling them with a microcomputer.

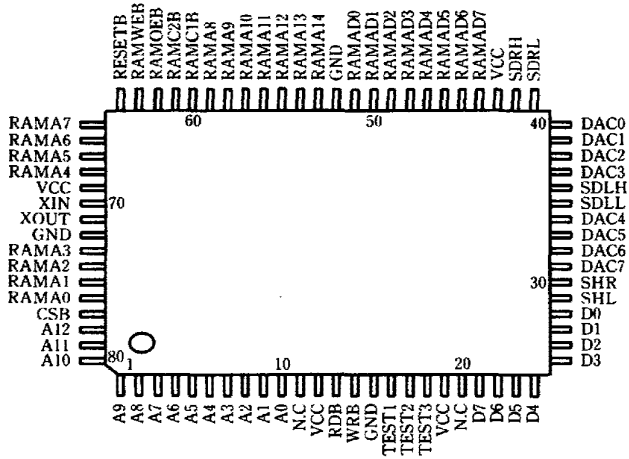
## ■ FEATURES

- PCM sound generation method
- Number of channels . . . . . 8
- Source clock frequency . . . . . 10 MHz max.
- Sampling frequency . . . . . 19.8 kHz (source clock = 7.6 MHz)
- Waveform data width . . . . . 8 bits
- Number of waveform words . . . . . Any
- Waveform memory space . . . . . 64 K-bytes max.
- Envelope data width . . . . . 8 bits
- Left(L) and Right(R) stereo output at arbitrary orientation level
- Pitch fine adjustment
- Interface with 8-bit CPUs
- Interface with waveform memories
  - Can be directly coupled with two 256K (32K × 8) pseudo SRAMs.
  - Can be directly coupled with two 256K (32K × 8) mask ROMs.
  - Can be directly coupled with two 256K (32K × 8) SRAMs.
- Interface with D/A converters
  - Can be directly coupled with 10-bit serial D/A converters.
  - Can be directly coupled with 8-bit parallel D/A converters.
- Silicon gate CMOS process
- 5V single power supply
- Package . . . . . 80-pin flat package.

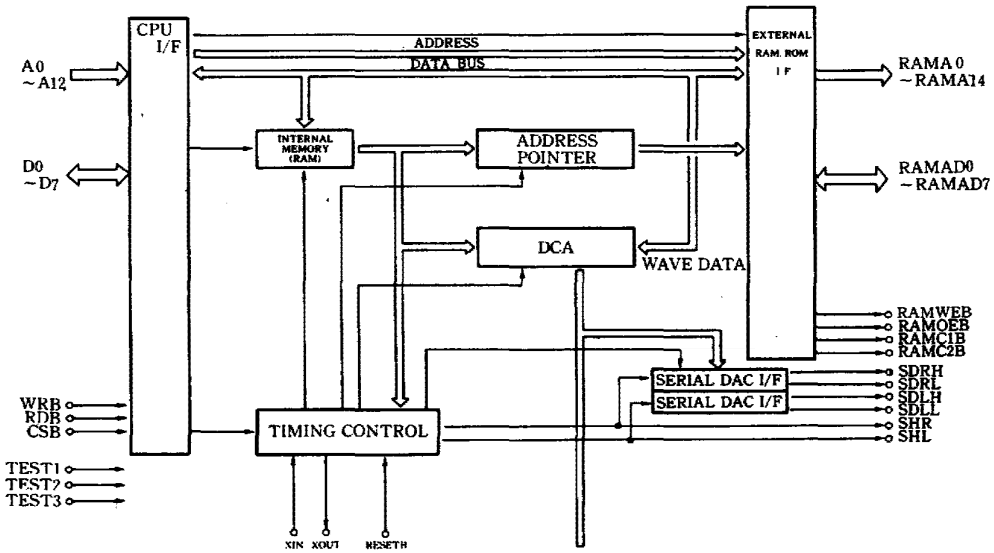
## ■ APPLICATIONS

Sound generator for personal computers, electronic instruments, TV games, and toys.

## ■ PIN CONFIGURATION (Top View)



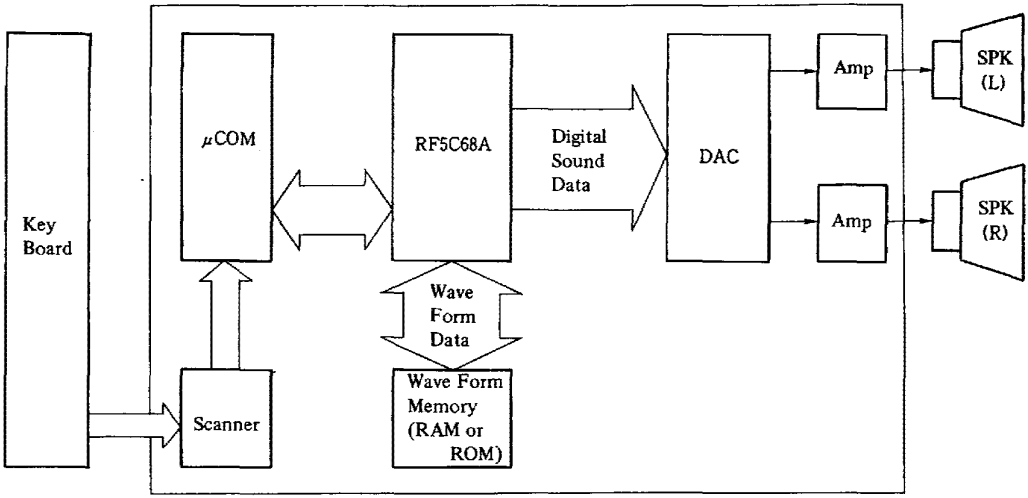

## ■ BLOCK DIAGRAM



## ■ PIN DESCRIPTION

| PIN NAME | FUNCTION | I/O | DESCRIPTION |
|---|---|---|---|
| A0 ~ A12 | Address input | I | Address signals input from a microcomputer . |
| D0 ~ D17 | Data input output | I/O | Data bus signals between RF5C68A and a microcomputer |
| CSB | Chip select input | I | Chip select signals input from a microcomputer |
| RDB | Read enable input | I | Read signals input from a microcomputer |
| WRB | Write enable input | I | Write signals input from a microcomputer |
| RAMAD0 ~ RAMAD7 | RAM address input output | I/O | When pseudo SRAMs are connected, these are multiplex signals of lower addresses/data between RF5C68A and SRAMs. When MROMs are connected, these are data input signals from MROMs.<br>When SRAMs are connected, these are data bus signals between RF5C68A and SRAMs. |
| RAMA8 ~ RAMA14 | RAM address output | O | Higher address signals of SRAM and MROM |
| RAMA0 ~ RAMA7 | RAM address output | O | Lower address signals of SRAM and MROM |
| RAMC2B | Memory select output | O | SRAM and MROM select signals of higher 32 K-bytes |
| RAMC1B | Memory select output | O | SRAM and MROM select signals of lower 32 K-bytes |
| RAMWEB | RAM write enable output | O | Write signals of pseudo SRAM and SRAM |
| RAMOEB | Memory output enable output | O | Read signals of pseudo SRAM, SRAM, and MROM |
| SDLH | Higher "L" data output | O | Higher "L" data signals output to serial DACs |
| SDLL | Lower "L" data output | O | Lower "L" data signals output to serial DACs |
| SDRH | Higher "R" data output | O | Higher "R" data signals output to serial DACs |
| SDRL | Lower "R" data output | O | Lower "R" data signals output to serial DACs |
| DAC0 ~ DAC7 | Multiplex signal output | O | "R" data/"L" data multiplex signals output to parallel DACs |
| SHL | "L" data sample/hold signals output | O | "L" data sample/hold signals of DAC0 to DAC7 |
| SHR | "R" data sample/hold signals output | O | "R" data sample/hold signals of DAC0 to DAC7 |
| RESETB | Reset signals input | I | Reset signals |
| XIN | Crystal signals input | I | External terminal of crystal oscillator<br>Clock can be directly input to XIN. |
| XOUT | Crystal signals output | O | |
| TEST 1<br>TEST 2<br>TEST 3 | Test input pin | I | These are test inputs usually set to logic "L".<br>When MROM or SRAM is used for memory, TEST2 is set to logic "H". |
| VCC | Power supply | – | Power supply terminal |
| GND | Ground | – | Grounding terminal |

## ■ APPLICATION EXAMPLE




## ■ ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Condition | Limit | Unit |
|---|---|---|---|---|
| Vcc | Supply voltage | GND = 0V | −0.3 ~ 7 | V |
| VTE | Input and Output Voltage | GND = 0V | −0.3 ~ Vcc + 0.3 | V |
| Pd | Maximum Power consumption | | 200 | mW |
| Topr | Operating Ambient Temperature | | 0 ~ 70 | °C |
| Tstg | Storage Temperature | | −40 ~ 125 | °C |

## ■ RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Specified Value | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ. | Max. | |
| Vcc | Supply Voltage | 4.5 | | 5.5 | V |
| VIH | Input High Voltage | 2.2 | | Vcc + 0.3 | V |
| VIL | Input Low Voltage | −0.3 | | 0.8 | V |
| Ta | Ambient Temperature | 0 | | 70 | °C |

## ■ DC CHARACTERISTICS

(Ta = 0 ~ 70°C, Vcc = 5V ± 10%)

| Symbol | Parameter | Test Condition | Specified Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{IH1}$ | Input High Voltage (TTL Compatible) | | 2.0 | | Vcc + 0.3 | V |
| $V_{IL1}$ | Input Low Voltage (TTL Compatible) | | −0.3 | | 0.8 | V |
| $V_{IH2}$ | Input High Voltage (XIN pin) | | 3.5 | | Vcc + 0.3 | V |
| $V_{IL2}$ | Input Low Voltage (XIN pin) | | −0.3 | | 1.5 | V |
| $I_{LI}$ | Input Leakage Current | $0v \leqq V_{IN} \leqq Vcc$ | −10 | | 10 | μA |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = −4.0 mA | 2.4 | | | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 4.0 mA | | | 0.4 | V |
| $I_{OZ}$ | Output Leakage Current for OFF State | $0v \leqq V_{OUT} \leqq Vcc$ | −10 | | 10 | μA |
| $I_{CC0}$ | Standby Supply Current | $V_{IN}$ = 0V, Vcc | | | 300 | μA |
| $I_{CC1}$ | Operating Supply Current | $f_{OPR}$ = 10 MHz | | | 30 | mA |

## ■ AC CHARACTERISTICS

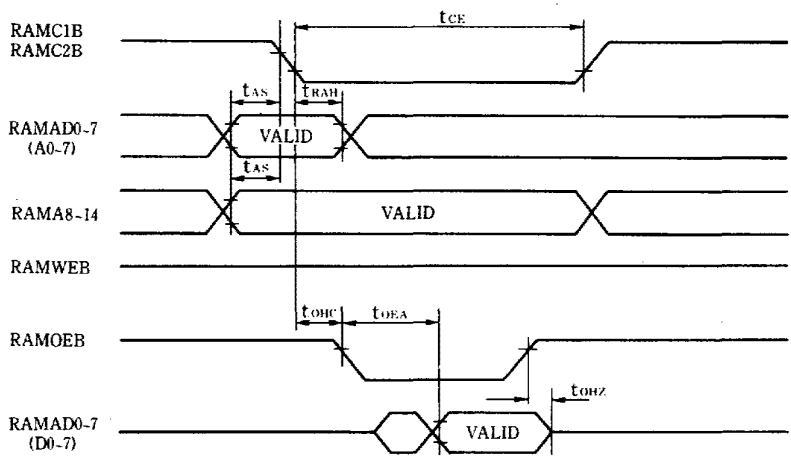
(Ta = 0 ~ 70°C, Vcc = 5V ± 10%)

| Symbol | Parameter | Test Condition | Specified Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $f_{OPR}$ | Input Clock Frequency | | | | 10 | MHz |
| $T_{CE}$ | RAMCE 1, 2 Pulse Width | | 200 | | | ns |
| $T_{AS}$ | Address to RAMCE 1, 2 | | 0 | | | ns |
| $T_{RAH}$ | RAMCE 1, 2 to Row Address | | 30 | | | ns |
| $T_{OHC}$ | RAMCE 1, 2 to RAMOEB | | 0 | | | ns |
| $T_{OEA}$ | RAMOEB to Read Data Valid | | | | 50 | ns |
| $T_{OHZ}$ | RAMOEB to Read Data Float | | 20 | | | ns |
| $T_{CW}$ | RAMCE 1, 2 to RAMWEB High | | 200 | | | ns |
| $T_{WP}$ | RAMWEB Pulse Width | | 35 | | | ns |
| $T_{DW}$ | Write-Data Valid to RAMWEB High | | 30 | | | ns |
| $T_{DH}$ | Write-Data Hold after RAMWEB High | | 0 | | | ns |
| $T_{RDA}$ | Read-Data Valid to RDB High | | | | 100 | ns |
| $T_{RDH}$ | Read-Data Hold after RDB High | | 10 | | | ns |
| $T_{WRH}$ | Write-Data Valid to WRB High | | 30 | | | ns |
| $T_{WRH}$ | Write-Data Hold after WRD High | | 30 | | | ns |

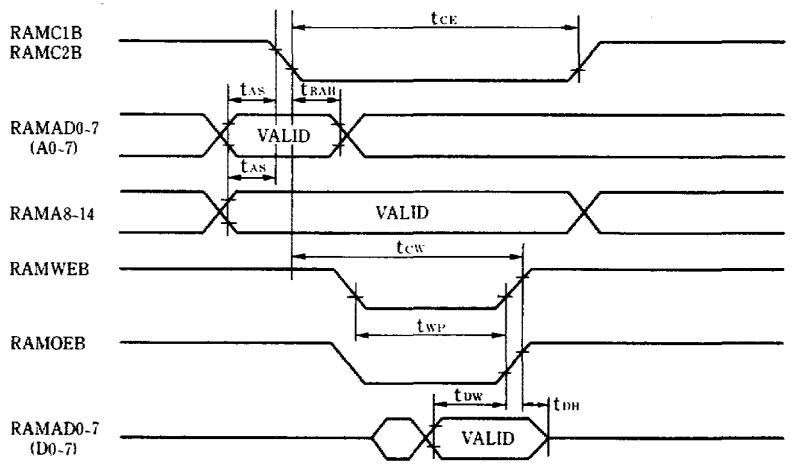
## ■ TIMING CHART

### 1. Psendo SRAM Interface

* Read Cycle

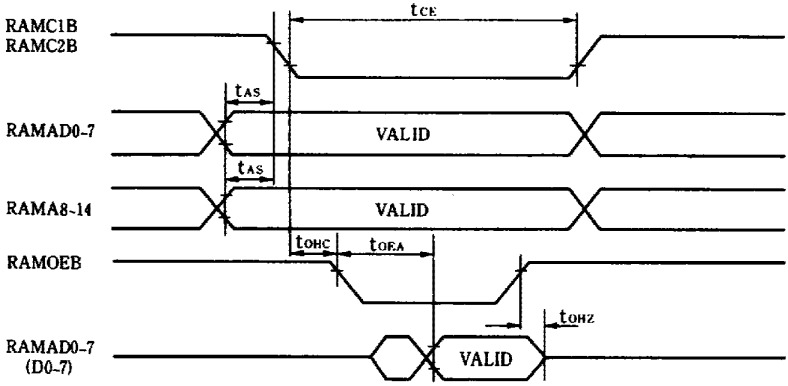



* Write Cycle



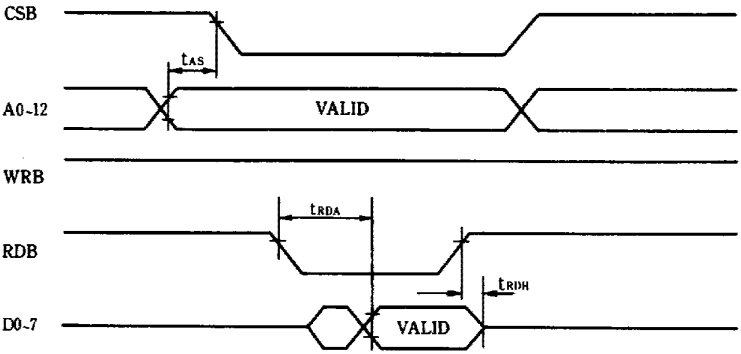
2. **Mask ROM Interface**

* Read Cycle

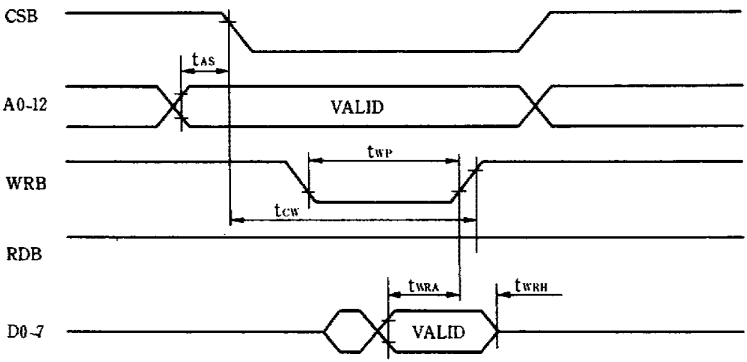



3. **CPU Interface**

* Read Cycle




* Write Cycle



## ■ FUNCTIONS

### 1. PCM Sound Generation

Waveform data (WAVE DATA) is specified by the internal address pointer of RF5C68A, and is read from external waveform memories. RF5C68A multiplies it with envelope data (ENV DATA) or stereo pan pot data (PAN DATA) that are stored in the internal memory (RAM). The operation above is performed for each of the eight channels. RF5C68A outputs the total of the results as single-sample PCM sound data (digital data).

RF5C68A performs the operation even to the channel that is not sounding. Therefore, one sampling requires a fixed time (one cycle of source clock × 384).

However, the operation result of the channel that is not sounding does not affect the output PCM sound data.

The digital control amplifier (DCA) block, which executes the above processing, is described below.

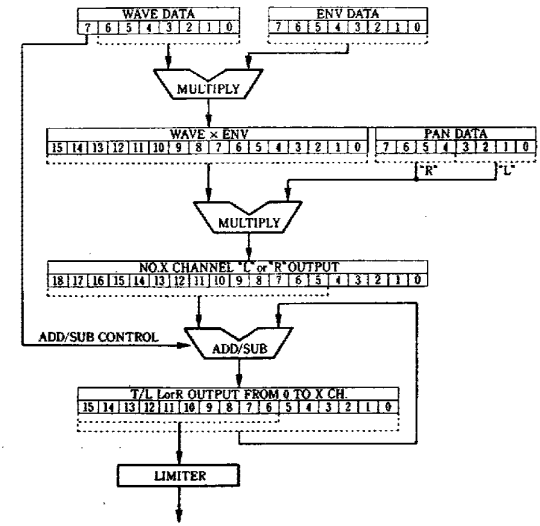
**[DCA block]**

The digital control amplifier block generates musical tones using the data read from internal and external memories.

The figure below shows how each type of data is processed.

The above processing is performed sequentially for each of the channels 1 to 8. Every time the R and L outputs of the eight channels are totaled, sample/hold signals for R and L are generated.

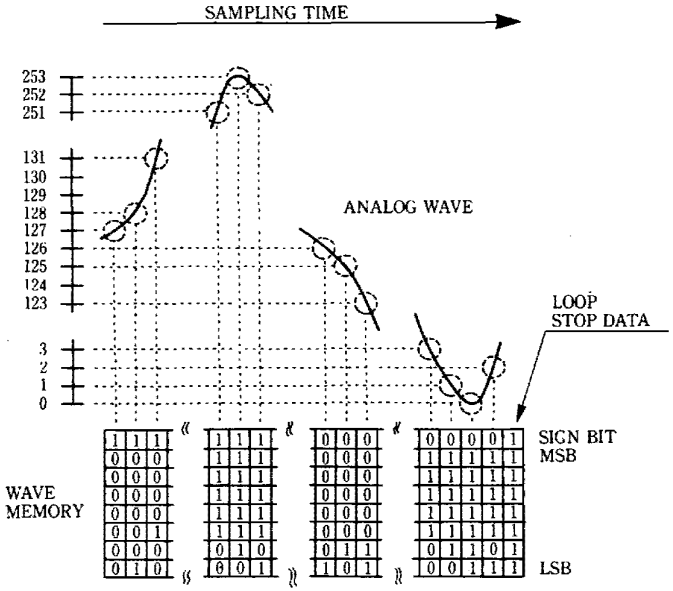
If there is a plus side overflow while totaling the values of the eight channels, the limiter circuit sets FFFFH as the result. If there is a minus side overflow, the limiter sets 0000H as the result.



**[Example of waveform data format]**

The figure below shows an example format of waveform data to be stored in an external waveform memory. In this example, digital sampling is performed assuming that the values of the analog waveform are 127 at the center, 253 at maximum, and 0 at minimum.

The 'FFH' waveform data is handled as loop stop data (therefore, 'FFH' cannot be used as waveform data). If 'FFH' data is read from the waveform memory, the waveform memory read address is reset to the LSH and LSL data (see 2. Wave Form Memory Read), and waveform data is read again.



**2. Wave Form Memory Read**

RF5C68A has an address pointer that specifies addresses of a 64K-byte waveform memory independently for eight channels, according to start address data (ST data), loop start address data (LSH data, LSL data), and address count data (FDH data, FDL data) that are stored in the internal memory, and loop stop data that is stored in the waveform memory.

The address pointer fixes the waveform memory read address of a channel that is not sounding to the ST data of that channel. Therefore, in the first sampling cycle after the channel has started sounding, music tones are always read from the waveform memory specified by the ST data.

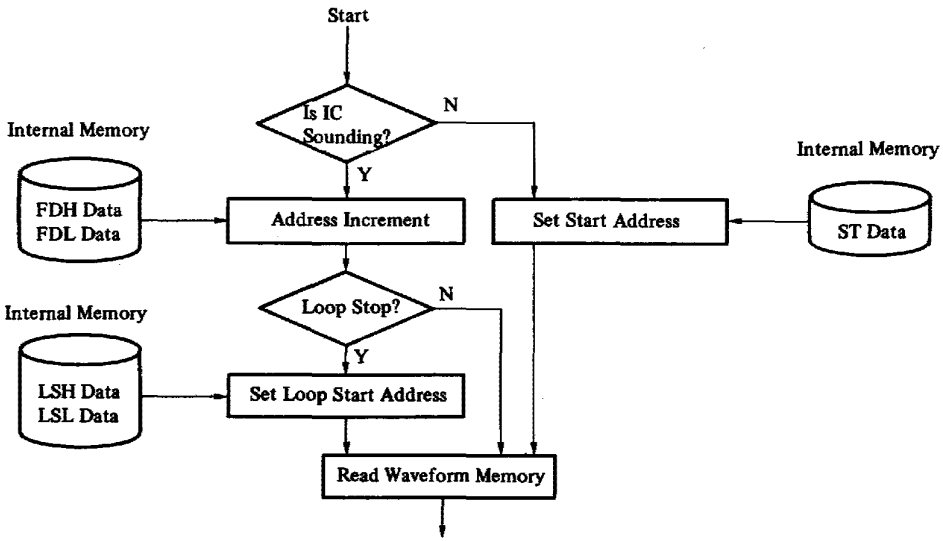
Waveform memories are read after the waveform memory address which has been sampled previously by the sounding channel is incremented according to FDH and FDL data of that channel.

The waveform memory is read after its address which has been smapled previously by the sounding channel is incremented according to FDH and FDL data of that channel. Therefore, the music tone data stored in the waveform memory can be set to any frequency.

If the loop stop data (FFH) stored in the waveform memory is read, waveform memory read address is set to the LSH and LSL data, and the waveform memory is read again. Therefore, any part of music tone data stored in the waveform memory can sound repeatedly.

**[Address pointer function]**

The address pointer controls addresses of 11 digits below the decimal point, for fine-adjusting the integer address to specify addresses of the 64K-byte waveform memory and the music tone frequency. The flow-chart below shows the processing executed independently for each of the eight channels.



**[Example of music tone data frequency setting]**

Examples of FDH and FDL setting are shown below.

[Number of timbre data words: 256 words
Source clock frequency: 10 MHz]

| Timbre name | FD set value | | Frequency responding to the FD set value (Hz) | Voice | FD set value | | Frequency responding to the FD set value (Hz) |
|---|---|---|---|---|---|---|---|
| | FDH | FDL | | | FDH | FDL | |
| $C_1$ | 02 | 92 | 32.68 | $C_4$ | 14 | 93 | 261.61 |
| $C_1$ | 02 | B9 | 34.62 | $C_4$ | 15 | D4 | 277.56 |
| $D_1$ | 02 | E3 | 36.71 | $D_4$ | 17 | 18 | 293.65 |
| $D_1$ | 03 | 0E | 38.84 | $D_4$ | 18 | 77 | 311.09 |
| $E_1$ | 03 | 3D | 41.18 | $E_4$ | 19 | EC | 329.61 |
| $F_1$ | 03 | 6E | 43.61 | $F_4$ | 1B | 76 | 349.18 |
| $F_1$ | 03 | A3 | 46.24 | $F_4$ | 1D | 18 | 369.95 |
| $G_1$ | 03 | DA | 48.98 | $G_4$ | 1E | D4 | 392.00 |
| $G_1$ | 04 | 15 | 51.91 | $G_4$ | 20 | A9 | 415.30 |
| $A_1$ | 04 | 53 | 54.99 | $A_4$ | 22 | 9A | 439.98 |
| $A_1$ | 04 | 95 | 58.26 | $A_4$ | 24 | A9 | 466.16 |
| $B_1$ | 04 | DA | 61.69 | $B_4$ | 26 | D7 | 493.87 |
| $C_2$ | 05 | 24 | 65.37 | $C_5$ | 29 | 26 | 523.23 |
| $C_2$ | 05 | 72 | 69.24 | $C_5$ | 2B | 98 | 554.32 |
| $D_2$ | 05 | C5 | 73.36 | $D_5$ | 2E | 30 | 587.30 |
| $D_2$ | 06 | 1D | 77.73 | $D_5$ | 30 | EF | 622.22 |
| $E_2$ | 06 | 7A | 82.35 | $E_5$ | 33 | D8 | 659.23 |
| $F_2$ | 06 | DD | 87.27 | $F_5$ | 36 | ED | 698.42 |
| $F_2$ | 07 | 46 | 92.49 | $F_5$ | 3A | 31 | 739.94 |
| $G_2$ | 07 | B5 | 98.00 | $G_5$ | 3D | A7 | 783.95 |
| $G_2$ | 08 | 2A | 103.81 | $G_5$ | 41 | 52 | 830.59 |
| $A_2$ | 08 | A6 | 109.97 | $A_5$ | 45 | 34 | 879.96 |
| $A_2$ | 09 | 2A | 116.53 | $A_5$ | 49 | 52 | 932.32 |
| $B_2$ | 09 | B5 | 123.43 | $B_5$ | 4D | AE | 987.75 |
| $C_3$ | 0A | 49 | 130.78 | $C_6$ | 52 | 4C | 1046.5 |
| $C_3$ | 0A | E6 | 138.58 | $C_6$ | 57 | 31 | 1108.7 |
| $D_3$ | 0B | 8C | 146.83 | $D_6$ | 5C | 61 | 1174.7 |
| $D_3$ | 0C | 3B | 155.52 | $D_6$ | 61 | DF | 1244.5 |
| $E_3$ | 0C | F6 | 164.81 | $E_6$ | 67 | B0 | 1318.5 |
| $F_3$ | 0D | BB | 174.59 | $F_6$ | 6D | D3 | 1396.5 |
| $F_3$ | 0E | 8C | 184.97 | $F_6$ | 74 | 64 | 1480.0 |
| $G_3$ | 0F | 6A | 196.00 | $G_6$ | 7B | 50 | 1568.0 |
| $G_3$ | 10 | 54 | 207.62 | $G_6$ | 82 | A4 | 1661.2 |
| $A_3$ | 11 | 4D | 219.99 | $A_6$ | 8A | 69 | 1760.0 |
| $A_3$ | 12 | 54 | 233.05 | $A_6$ | 92 | A5 | 1864.7 |
| $B_3$ | 13 | 6B | 246.91 | $B_6$ | 9B | 60 | 1975.7 |
| | | | | $C_7$ | A4 | 99 | 2093.0 |

### 3. Internal Data Setting

(1) Address map

There is an 8K byte address space inside that can be accessed from a microcomputer. The table below shows the address map.

| [ Address ] | [ Content ] |
|---|---|
| 1FFFH<br><br>1000H | Waveform data<br>Waveform data memory is accessed via this IC. 4K byte can be directly accessed.<br>Using the bank function in the control Reg enables access to up to 64K byte. |
| 0FFFH<br><br>0009H | Not used |
| 0008H | Channel ON/OFF Reg |
| 0007H | Control Reg |
| 0006H | *ST data memory |
| 0005H | *LSH data memory |
| 0004H | *LSL data memory |
| 0003H | *FDH data memory |
| 0002H | *FDL data memory |
| 0001H | *PAN data memory |
| 0000H | *ENV data memory |

* : Items marked with * must be set independently for each channel by the bank function in the control Reg.

(2) Control Reg

This register sets modes of this IC, waveform memory bank addresses, and internal memory bank channels.

This is a write-only register.

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Bit |
|---|---|---|---|---|---|---|---|---|
| ON<br>OFF | MOD | – | – | *WB3 | WB2 | WB1 | WB0 | Address |
| | | | | – | CB2 | CB1 | CB0 | 0007H |

*WB: Wave bank

Bit 7: ON/OFF

This IC starts sounding when this bit is set and stops sounding when this bit is reset. External waveform memories of a microcomputer can be read only when the IC is not sounding. When the IC is sounding, writing to the external waveform memories is restricted as described later.

Bit 6: MOD

This bit controls to which register the content of bits 3 to 0 is written.

The microcomputer writes the content of bits 2 to 0 to CBs 2 to 0 when this bit is "H", and writes the content of bits 3 to 0 to WBs 3 to 0 when this bit is "L"

When MOD = 'H'

Bits 2 to 0: CBs* 2 to 0

These bits control selection of channels when the microcomputer accesses internal memories (ENV, PAN, FDL, FDH, LSL, LSH, and ST).

*CB: Channel Bank

| CB 2 | CB 1 | CB 0 | Channel NO. |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 2 |
| 0 | 1 | 0 | 3 |
| 0 | 1 | 1 | 4 |
| 1 | 0 | 0 | 5 |
| 1 | 0 | 1 | 6 |
| 1 | 1 | 0 | 7 |
| 1 | 1 | 1 | 8 |

When MOD = 'L'

Bits 3 to 0: WBs 3 to 0

These bits control higher addresses when the micro computer accesses external waveform memories.

The table below shows the relation between set values of WBs 3 to 0 and the addresses for accessing external waveform memories.

| WB 3 | WB 2 | WB 1 | WB 0 | External waveform memory address | |
|---|---|---|---|---|---|
| | | | | Memory No. | Address |
| 0 | 0 | 0 | 0 | 1 | 0000H~0FFFH |
| 0 | 0 | 0 | 1 | 1 | 1000H~1FFFH |
| 0 | 0 | 1 | 0 | 1 | 2000H~2FFFH |
| 0 | 0 | 1 | 1 | 1 | 3000H~3FFFH |
| 0 | 1 | 0 | 0 | 1 | 4000H~4FFFH |
| 0 | 1 | 0 | 1 | 1 | 5000H~5FFFH |
| 0 | 1 | 1 | 0 | 1 | 6000H~6FFFH |
| 0 | 1 | 1 | 1 | 1 | 7000H~7FFFH |
| 1 | 0 | 0 | 0 | 2 | 0000H~0FFFH |
| 1 | 0 | 0 | 1 | 2 | 1000H~1FFFH |
| 1 | 0 | 1 | 0 | 2 | 2000H~2FFFH |
| 1 | 0 | 1 | 1 | 2 | 3000H~3FFFH |
| 1 | 1 | 0 | 0 | 2 | 4000H~4FFFH |
| 1 | 1 | 0 | 1 | 2 | 5000H~5FFFH |
| 1 | 1 | 1 | 0 | 2 | 6000H~6FFFH |
| 1 | 1 | 1 | 1 | 2 | 7000H~7FFFH |

**Note:** Memory No. 1 is selected by RAMC1B.
Memory No. 2 is selected by RAMC2B.

(3) Internal memory

This internal memory stores data for sounding, which will be described later, for each of the eight channels.

a. ST data ..... (Address = 0006H) For the address of the waveform memory read of a channel that starts sounding, the higher eight bits are the ST data that responds to the channel. 'OOH' is set to the lower address.

b. LSH data ..... (Address = 0005H) When the stop data is read from the waveform memory while the IC is sounding, its lower address is converted into LSH data, and the waveform memory is read again.

c. LSL data ..... (Address = 0004H) When the stop data is read from the waveform memory while the IC is sounding, its lower address is converted into LSL data, and the waveform memory is read again.

d. FDH data ..... (Address = 0003H) This data controls the address counter that indicates the address to be read from the waveform memory while the IC is sounding.

Setting arbitrary bits of FDH enables address increment of one sampling time as shown in the table below.

| FDH bit | Address increment |
|---|---|
| 7 | $2^4$ |
| 6 | $2^3$ |
| 5 | $2^2$ |
| 4 | $2^1$ |
| 3 | $2^0$ |
| 2 | $2^{-1}$ |
| 1 | $2^{-2}$ |
| 0 | $2^{-3}$ |

**Example:** When only bits 4 and 3 of FDH are set, the address is incremented by $2^1 + 2^0 = 3$ counts in one sampling.

e. FDL data ..... (Address = 0002H) This data controls the address counter that indicates the address to be read from the waveform memory while the IC is sounding.

Setting arbitrary bits of FDL enables address increment of one sampling time as shown on the next page.

| FDL bit | Address increment |
|---|---|
| 7 | $2^{-4}$ |
| 6 | $2^{-5}$ |
| 5 | $2^{-6}$ |
| 4 | $2^{-7}$ |
| 3 | $2^{-8}$ |
| 2 | $2^{-9}$ |
| 1 | $2^{-10}$ |
| 0 | $2^{-11}$ |

**Example:** When only bits 4 and 3 of FDL are set, the address is incremented by $2^{-7} + 2^{-8}$ counts in one sampling.

f. PAN data ..... This data controls the separation of output generated from the sounding channel into 'L' and 'R' stereo outputs.
(Address = 0001H)

The higher four bits of PAN data are the coefficient of the 'R' output, and the lower four bits are that of the 'L' output.

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Bit |
|---|---|---|---|---|---|---|---|---|
| MSB | | | LSB | MSB | | | LSB | Address |
| Coefficient of the 'R' output | | | | Coefficient of the 'L' output | | | | 0001H |

g. ENV data ..... To vary the amplitude of the waveform data read from the waveform memory by the sounding channel, this data multiplies it with the ENV data.
(Address = 0001H)

Bit 7 is MSB, and bit 0 is LSB.

(4) Channel ON/OFF Reg

This register controls start/stop of sounding for each channel.
However, the control by the control register is given priority, and this register is valid when the control register sets the sounding state.

Bit 0 responds to channel 1, and bit 7 responds to channel 8.

## 4. Interface with Peripheral Devices

(1) Microcomputer interface

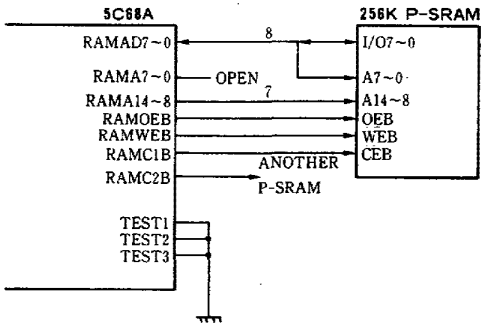
This IC can be used as a peripheral device of an 8-bit CPU.

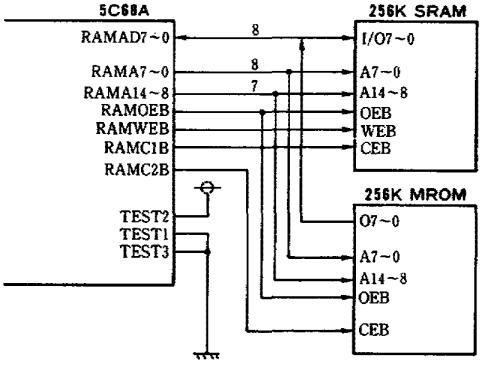
The control Reg's setting of sounding/not sounding states changes the conditions of the access from the microcomputer to this IC. See the table below.

| Condition | External waveform memory | | Internal memory | |
|---|---|---|---|---|
| | Read | Write | Read | Write |
| Sounding | Impossible | Access by cycles more than the 16 cycles of the source clock. | Impossible | Possible |
| Stopping | Possible | Possible | Impossible | Possible |

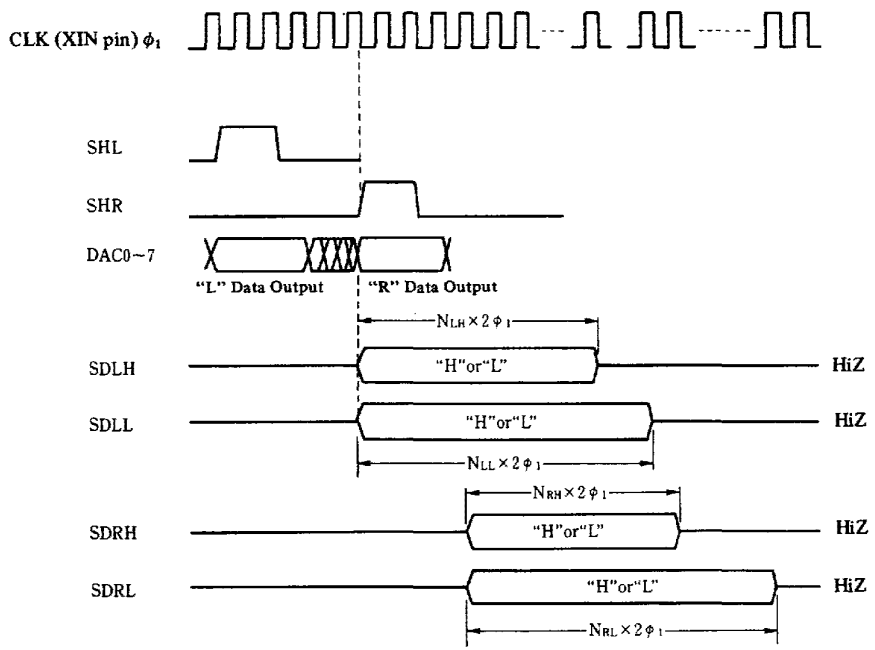
(2) Waveform memory interface

This IC externally connects pseudo SRAMs, SRAMs, or MROMs as waveform memories. Examples are shown in the figure below.



(3) RF5C68A outputs PCM sounds in digital values, and must have an external D/A converter connected. The output timing chart is shown below.

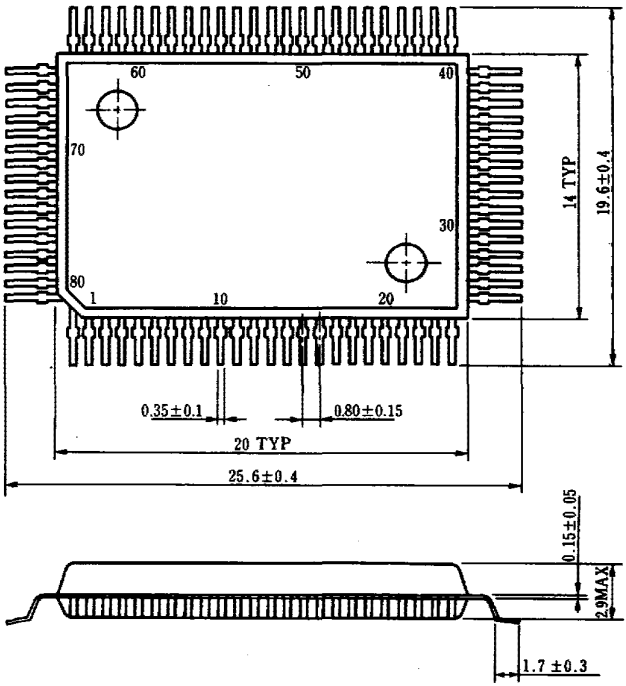



However, NLH, NLL, NRH, and NRL are the number of bits of the absolute value of the difference of the previous sound data. If it is larger than the previous data, the output value is "H", and if it is smaller, the output value is "L"

**[Example]**

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | $a_9$ | $a_8$ | $a_7$ | $a_6$ | $a_5$ | $a_4$ | $a_3$ | $a_2$ | $a_1$ | $a_0$ | ← Previous sound data (10 bits) |
| − | $b_9$ | $b_8$ | $b_7$ | $b_6$ | $b_5$ | $b_4$ | $b_3$ | $b_2$ | $b_1$ | $b_0$ | |
| | $c_9$ | $c_8$ | $c_7$ | $c_6$ | $c_5$ | $c_4$ | $c_3$ | $c_2$ | $c_1$ | $c_0$ | ← Absolute value of the sound data difference |
| | NLH or NRH | | | | | NLL or NRL | | | | | |

## ■ PACKAGE DIMENSION




Unit: mm