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Sega Enterprises, Ltd.
This service manual includes data for the GENESIS II and MEGA DRIVE II.

- Parts of the circuits are different in the GENESIS II depending on the model of IC11 (RGB encoder used). Check the model of IC11 on the main circuit board and identify the type, F, S or SM.

<table>
<thead>
<tr>
<th>Type</th>
<th>Model of IC11</th>
<th>Part No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>F</td>
<td>IC MB3514PF-G-BND-EF</td>
<td>313-5232-A</td>
</tr>
<tr>
<td>S</td>
<td>IC CXA1145M-T6 SOP</td>
<td>313-5213-A</td>
</tr>
<tr>
<td>SM</td>
<td>IC KA2195D</td>
<td>313-5236-A</td>
</tr>
</tbody>
</table>

- Differences in the circuits are shown in the difference tables in the schematic and circuit board diagrams.
- In the parts list, differences are shown in the REMARKS columns.
## 1. SPECIFICATIONS

### RATINGS

<table>
<thead>
<tr>
<th>Model</th>
<th>GENESIS II</th>
<th>MEGA DRIVE II</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>PAL-I</td>
</tr>
<tr>
<td>Power input</td>
<td>AC 120V, 60Hz</td>
<td>AC 220V, 50Hz,</td>
</tr>
<tr>
<td>Power consumption</td>
<td>18 W</td>
<td>18 W</td>
</tr>
<tr>
<td>Usable temperature</td>
<td>Humidity 5-35 ℃, 20-80%RH (non-condensing)</td>
<td></td>
</tr>
<tr>
<td>Dimensions</td>
<td>220 (W) x 212 (D) x 59 (H) mm</td>
<td></td>
</tr>
</tbody>
</table>

### SPECIFICATIONS

<table>
<thead>
<tr>
<th>CPU</th>
<th>68000 (8M) &amp; Z80A (4M)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memories</td>
<td>RAM 72k bytes</td>
</tr>
<tr>
<td></td>
<td>VRAM 64k bytes</td>
</tr>
<tr>
<td>Audio</td>
<td>FM, PSG, PCM</td>
</tr>
<tr>
<td>Display capability</td>
<td>VDP SEGA custom LSI</td>
</tr>
<tr>
<td></td>
<td>Display Regular color TV</td>
</tr>
<tr>
<td></td>
<td>Colors 512</td>
</tr>
<tr>
<td></td>
<td>Video outputs VIDEO RGB</td>
</tr>
<tr>
<td>Control terminals</td>
<td>2, control pad, etc. can be attached</td>
</tr>
<tr>
<td>Reset button</td>
<td>Game restart function</td>
</tr>
<tr>
<td>Slots</td>
<td>For cartridge and extension</td>
</tr>
</tbody>
</table>

* Design and specifications are subject to change without notice.*
2. IDENTIFYING PARTS

2-1. FRONT & TOP VIEW OF CONSOLE

CONSOLE

Cartridge Slot
Reset Button
Directional Button (D-Button)
Control Port 2
Control Port 1
Power Button

CONTROL PAD

Start Button
Button C
Button B
Button A

2-2. BACK VIEW OF CONSOLE

Reverse Side
A/V OUT Jack
AC Adaptor Jack
Extension Compartment
A/V OUT ADAPTOR
2-3. ACCESSORIES

GENESIS II

RF Unit

AC Adaptor

MEGA DRIVE II

RF Unit

Peritel Cable

Sega 16-bit Game Cartridge

(Except French model)

(French model only)

(Provided or Sold separately)

AC Adaptor

(Except U.K.
Australis and New Zealand)

(U.K.)

(Australia and New Zealand)
3. DISASSEMBLY

3-1. Dismantling procedure
Removal of bottom screws and top case
1) Turn the power button off.
2) Turn the unit over. (See Fig. 1)
3) Remove four screws (202).
4) Remove top case (1).

Main board removal (See Fig. 2)
1) Remove nine screws (201).
2) Remove the shield plate.
3) Remove two screws (203).
4) Remove the main board from the bottom case (2).

3-2. Reinstalling procedure
Main board reinstallation
1) Attach the 64-pin cover (8).
2) Attach the main board to the bottom case.
3) Tighten two screws (203).
4) Attach the shield plate.
5) Tighten nine screws (201).

Top case reinstallation
1) Turn off the tactile power switch (TACT SW) on the main board.
2) Attach the top case.
3) Engage the top case with the bottom case.

Tightening the screws on the bottom case.
1) Turn the unit over. (See Fig. 1)
2) Tighten four screws (202).
*DIFFERENCE TABLE FOR DIAGRAM-1*

<table>
<thead>
<tr>
<th>CIRCUIT No.</th>
<th>GRID</th>
<th>GENESIS II</th>
<th>MEGA DRIVE II</th>
</tr>
</thead>
<tbody>
<tr>
<td>OSC1</td>
<td>C-5</td>
<td>53.693175MHz</td>
<td>53.203424MHz</td>
</tr>
<tr>
<td>C9</td>
<td>E-7</td>
<td>NOT USED</td>
<td>47P</td>
</tr>
<tr>
<td>C10</td>
<td>C-5</td>
<td>NOT USED</td>
<td>10P</td>
</tr>
<tr>
<td>C11</td>
<td>B-4</td>
<td>NOT USED</td>
<td>33P</td>
</tr>
</tbody>
</table>

5-2. SCHEMATIC DIAGRAM-2
* DIFFERENCE TABLE FOR DIAGRAM-4

<table>
<thead>
<tr>
<th>CIRCUIT No.</th>
<th>GRID</th>
<th>GENESIS II TYPE-F</th>
<th>TYPE-S</th>
<th>TYPE-SM</th>
<th>MEGA DRIVE II</th>
</tr>
</thead>
<tbody>
<tr>
<td>IC11</td>
<td>E-6</td>
<td>MB3514PF-G-BND-EF</td>
<td>CXA1145-T6 SOP</td>
<td>KA2195D</td>
<td>MB3514PF-G-BND-EF</td>
</tr>
<tr>
<td>L2</td>
<td>E-7</td>
<td>100 µ</td>
<td>100 µ</td>
<td>NOT USED</td>
<td>100 µ</td>
</tr>
<tr>
<td>L3</td>
<td>D-7</td>
<td>12 µ</td>
<td>12 µ</td>
<td>NOT USED</td>
<td>10 µ</td>
</tr>
<tr>
<td>L6</td>
<td>D-7</td>
<td>NOT USED</td>
<td>NOT USED</td>
<td>NOT USED</td>
<td>100 µ</td>
</tr>
<tr>
<td>CE14</td>
<td>D-6</td>
<td>220 µ</td>
<td>10 µ</td>
<td>10 µ</td>
<td>220 µ</td>
</tr>
<tr>
<td>C28</td>
<td>E-7</td>
<td>18P (CH)</td>
<td>18P (CH)</td>
<td>NOT USED</td>
<td>18P (CH)</td>
</tr>
<tr>
<td>C29</td>
<td>D-7</td>
<td>0.01 µ</td>
<td>0.01 µ</td>
<td>NOT USED</td>
<td>0.01 µ</td>
</tr>
<tr>
<td>C30</td>
<td>D-7</td>
<td>180P (CH)</td>
<td>180P (CH)</td>
<td>NOT USED</td>
<td>180P (CH)</td>
</tr>
<tr>
<td>C32</td>
<td>E-6</td>
<td>15P (CH)</td>
<td>15P (CH)</td>
<td>NOT USED</td>
<td>15P (CH)</td>
</tr>
<tr>
<td>C57</td>
<td>D-5</td>
<td>100P (CH)</td>
<td>NOT USED</td>
<td>NOT USED</td>
<td>100P (CH)</td>
</tr>
<tr>
<td>C61</td>
<td>D-6</td>
<td>NOT USED</td>
<td>NOT USED</td>
<td>NOT USED</td>
<td>0.1 µ</td>
</tr>
<tr>
<td>C62</td>
<td>D-7</td>
<td>NOT USED</td>
<td>NOT USED</td>
<td>NOT USED</td>
<td>12P (CH)</td>
</tr>
<tr>
<td>R47</td>
<td>E-6</td>
<td>12K</td>
<td>1.2K</td>
<td>NOT USED</td>
<td>12K</td>
</tr>
<tr>
<td>R54</td>
<td>D-6</td>
<td>NOT USED</td>
<td>24K</td>
<td>24K</td>
<td>NOT USED</td>
</tr>
<tr>
<td>R55</td>
<td>D-6</td>
<td>10K</td>
<td>1K</td>
<td>NOT USED</td>
<td>10K</td>
</tr>
<tr>
<td>R56</td>
<td>D-7</td>
<td>1.2K</td>
<td>1.2K</td>
<td>NOT USED</td>
<td>1.2K</td>
</tr>
<tr>
<td>R57</td>
<td>D-7</td>
<td>330</td>
<td>330</td>
<td>NOT USED</td>
<td>1K</td>
</tr>
<tr>
<td>R61</td>
<td>E-5</td>
<td>4.7K</td>
<td>10K</td>
<td>10K</td>
<td>4.7K</td>
</tr>
</tbody>
</table>
6. CIRCUIT BOARD DIAGRAMS
6-1. MAIN CIRCUIT BOARD (Top View) — For GENESIS II —

*DIFFERENCE TABLE*

<table>
<thead>
<tr>
<th>CIRCUIT No.</th>
<th>TYPE-F</th>
<th>TYPE-S</th>
<th>TYPE-SM</th>
</tr>
</thead>
<tbody>
<tr>
<td>L2</td>
<td>O</td>
<td>O</td>
<td>x</td>
</tr>
<tr>
<td>L3</td>
<td>O</td>
<td>O</td>
<td>x</td>
</tr>
<tr>
<td>L6</td>
<td>x</td>
<td>x</td>
<td>x</td>
</tr>
<tr>
<td>C9</td>
<td>x</td>
<td>x</td>
<td>x</td>
</tr>
<tr>
<td>C10</td>
<td>x</td>
<td>x</td>
<td>x</td>
</tr>
<tr>
<td>C11</td>
<td>x</td>
<td>x</td>
<td>x</td>
</tr>
<tr>
<td>C28</td>
<td>o</td>
<td>O</td>
<td>x</td>
</tr>
<tr>
<td>C29</td>
<td>o</td>
<td>o</td>
<td>x</td>
</tr>
<tr>
<td>C30</td>
<td>o</td>
<td>o</td>
<td>x</td>
</tr>
<tr>
<td>C32</td>
<td>o</td>
<td>o</td>
<td>x</td>
</tr>
<tr>
<td>C57</td>
<td>o</td>
<td>x</td>
<td>x</td>
</tr>
<tr>
<td>C61</td>
<td>x</td>
<td>x</td>
<td>x</td>
</tr>
<tr>
<td>C62</td>
<td>x</td>
<td>x</td>
<td>x</td>
</tr>
<tr>
<td>R47</td>
<td>o</td>
<td>o</td>
<td>x</td>
</tr>
<tr>
<td>R54</td>
<td>x</td>
<td>o</td>
<td>o</td>
</tr>
<tr>
<td>R55</td>
<td>o</td>
<td>o</td>
<td>x</td>
</tr>
<tr>
<td>R56</td>
<td>o</td>
<td>o</td>
<td>x</td>
</tr>
<tr>
<td>R57</td>
<td>o</td>
<td>o</td>
<td>x</td>
</tr>
</tbody>
</table>

x : NOT MOUNTED
O : MOUNTED
6-2. MAIN CIRCUIT BOARD (Bottom View) — For GENESIS II —
6-3. MAIN CIRCUIT BOARD (Top View) —For MEGA DRIVE II—
# 7. PARTS SPECIFICATION

**IC1** IC HD68HC000CP8  IC MC68HC000FN8

**Parts No.** 315-0685-A  315-0686-A

## Outside View

### Description

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Name</th>
<th>I/O</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>N/C</td>
<td>-</td>
<td>N/C</td>
</tr>
<tr>
<td>2</td>
<td>DTACK</td>
<td>I/O</td>
<td>Data Transfer Acknowledge.</td>
</tr>
<tr>
<td>3</td>
<td>BGACK</td>
<td>I/O</td>
<td>Bus Grant Acknowledge.</td>
</tr>
<tr>
<td>4</td>
<td>BR</td>
<td>I/O</td>
<td>Bus Request.</td>
</tr>
<tr>
<td>5</td>
<td>CLK</td>
<td>I</td>
<td>Clock.</td>
</tr>
<tr>
<td>6</td>
<td>HALT</td>
<td>I/O</td>
<td>Halt.</td>
</tr>
<tr>
<td>7</td>
<td>VMA</td>
<td>O</td>
<td>Valid Memory Address.</td>
</tr>
<tr>
<td>8</td>
<td>E</td>
<td>O</td>
<td>Enable.</td>
</tr>
<tr>
<td>9</td>
<td>BERR</td>
<td>I/O</td>
<td>Bus Error.</td>
</tr>
<tr>
<td>10</td>
<td>N/C</td>
<td>-</td>
<td>N/C</td>
</tr>
<tr>
<td>11</td>
<td>FC2</td>
<td>O</td>
<td>Function Code Output 2.</td>
</tr>
<tr>
<td>12</td>
<td>FC0</td>
<td>O</td>
<td>Function Code Output 0.</td>
</tr>
<tr>
<td>13</td>
<td>A1</td>
<td>O</td>
<td>Address Bus 1.</td>
</tr>
<tr>
<td>14</td>
<td>A3</td>
<td>O</td>
<td>Address Bus 3.</td>
</tr>
<tr>
<td>15</td>
<td>A4</td>
<td>O</td>
<td>Address Bus 4.</td>
</tr>
<tr>
<td>16</td>
<td>A6</td>
<td>O</td>
<td>Address Bus 6.</td>
</tr>
<tr>
<td>17</td>
<td>A7</td>
<td>O</td>
<td>Address Bus 7.</td>
</tr>
<tr>
<td>18</td>
<td>A9</td>
<td>O</td>
<td>Address Bus 9.</td>
</tr>
<tr>
<td>19</td>
<td>N/C</td>
<td>-</td>
<td>N/C</td>
</tr>
<tr>
<td>20</td>
<td>A11</td>
<td>O</td>
<td>Address Bus 14.</td>
</tr>
<tr>
<td>21</td>
<td>A16</td>
<td>O</td>
<td>Address Bus 16.</td>
</tr>
<tr>
<td>22</td>
<td>A17</td>
<td>O</td>
<td>Address Bus 17.</td>
</tr>
<tr>
<td>23</td>
<td>A18</td>
<td>O</td>
<td>Address Bus 19.</td>
</tr>
<tr>
<td>24</td>
<td>A20</td>
<td>O</td>
<td>Address Bus 20.</td>
</tr>
<tr>
<td>26</td>
<td>A22</td>
<td>O</td>
<td>Address Bus 22.</td>
</tr>
<tr>
<td>27</td>
<td>DI3</td>
<td>I/O</td>
<td>Data bus 15.</td>
</tr>
<tr>
<td>28</td>
<td>DI2</td>
<td>I/O</td>
<td>Data bus 12.</td>
</tr>
<tr>
<td>29</td>
<td>DI1</td>
<td>I/O</td>
<td>Data bus 10.</td>
</tr>
<tr>
<td>30</td>
<td>D8</td>
<td>I/O</td>
<td>Data bus 8.</td>
</tr>
<tr>
<td>31</td>
<td>D7</td>
<td>I/O</td>
<td>Data bus 7.</td>
</tr>
<tr>
<td>32</td>
<td>D5</td>
<td>I/O</td>
<td>Data bus 5.</td>
</tr>
<tr>
<td>33</td>
<td>D4</td>
<td>I/O</td>
<td>Data bus 4.</td>
</tr>
<tr>
<td>34</td>
<td>D2</td>
<td>I/O</td>
<td>Data bus 2.</td>
</tr>
<tr>
<td>35</td>
<td>D1</td>
<td>I/O</td>
<td>Data bus 1.</td>
</tr>
<tr>
<td>36</td>
<td>AS</td>
<td>O</td>
<td>Address Strobe.</td>
</tr>
<tr>
<td>37</td>
<td>LDS</td>
<td>O</td>
<td>Lower Data Strobe.</td>
</tr>
<tr>
<td>38</td>
<td>BG</td>
<td>O</td>
<td>Bus Grant.</td>
</tr>
<tr>
<td>39</td>
<td>VCC</td>
<td>I</td>
<td>Power Input.</td>
</tr>
<tr>
<td>40</td>
<td>VSS</td>
<td>I</td>
<td>GND.</td>
</tr>
<tr>
<td>41</td>
<td>RES</td>
<td>I/O</td>
<td>Reset.</td>
</tr>
<tr>
<td>42</td>
<td>VPA</td>
<td>I</td>
<td>Valid Peripheral Address.</td>
</tr>
<tr>
<td>43</td>
<td>IPL2</td>
<td>I</td>
<td>Interrupt Priority Level 2.</td>
</tr>
<tr>
<td>44</td>
<td>IPL0</td>
<td>I</td>
<td>Interrupt Priority Level 0.</td>
</tr>
<tr>
<td>45</td>
<td>FC1</td>
<td>O</td>
<td>Function Code Output 1.</td>
</tr>
<tr>
<td>46</td>
<td>N/C</td>
<td>-</td>
<td>N/C</td>
</tr>
<tr>
<td>47</td>
<td>A1</td>
<td>O</td>
<td>Address Bus 2.</td>
</tr>
<tr>
<td>48</td>
<td>A5</td>
<td>O</td>
<td>Address Bus 5.</td>
</tr>
<tr>
<td>49</td>
<td>A7</td>
<td>O</td>
<td>Address Bus 8.</td>
</tr>
<tr>
<td>50</td>
<td>A10</td>
<td>O</td>
<td>Address Bus 10.</td>
</tr>
<tr>
<td>51</td>
<td>A11</td>
<td>O</td>
<td>Address Bus 11.</td>
</tr>
<tr>
<td>52</td>
<td>A12</td>
<td>O</td>
<td>Address Bus 12.</td>
</tr>
<tr>
<td>53</td>
<td>A13</td>
<td>O</td>
<td>Address Bus 15.</td>
</tr>
<tr>
<td>54</td>
<td>A18</td>
<td>O</td>
<td>Address Bus 18.</td>
</tr>
<tr>
<td>55</td>
<td>VCC</td>
<td>I</td>
<td>Power Input.</td>
</tr>
<tr>
<td>56</td>
<td>VSS</td>
<td>I</td>
<td>GND.</td>
</tr>
<tr>
<td>57</td>
<td>A12</td>
<td>O</td>
<td>Address Bus 23.</td>
</tr>
<tr>
<td>58</td>
<td>DI4</td>
<td>I/O</td>
<td>Data bus 14.</td>
</tr>
<tr>
<td>59</td>
<td>DI1</td>
<td>I/O</td>
<td>Data bus 11.</td>
</tr>
<tr>
<td>60</td>
<td>DI8</td>
<td>I/O</td>
<td>Data bus 9.</td>
</tr>
<tr>
<td>61</td>
<td>DI6</td>
<td>I/O</td>
<td>Data bus 6.</td>
</tr>
<tr>
<td>62</td>
<td>DI3</td>
<td>I/O</td>
<td>Data bus 3.</td>
</tr>
<tr>
<td>63</td>
<td>DI7</td>
<td>I/O</td>
<td>Data bus 0.</td>
</tr>
<tr>
<td>64</td>
<td>UDS</td>
<td>O</td>
<td>Upper Data Strobe.</td>
</tr>
<tr>
<td>65</td>
<td>R/W</td>
<td>O</td>
<td>Read/Write.</td>
</tr>
<tr>
<td>66</td>
<td>IPL1</td>
<td>I</td>
<td>Interrupt Priority Level 1.</td>
</tr>
<tr>
<td>68</td>
<td>DI3</td>
<td>I/O</td>
<td>Data Bus 13.</td>
</tr>
</tbody>
</table>
IC2/3
IC HM65256BLFP-10
Parts No.: 315-0547-10A
IC TC81832AFL-10
Parts No.: 315-0677-A
IC TC51832FL-10
Parts No.: 315-0677-A
IC TC51832AFL-85
Parts No.: 315-0759-85A
IC LH5P832N-12
Parts No.: 315-0760-12A

■ Outside View

■ Pin Layout

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A. 1</td>
<td>VCC</td>
</tr>
<tr>
<td>A. 2</td>
<td>28 VCC</td>
</tr>
<tr>
<td>A. 3</td>
<td>WE</td>
</tr>
<tr>
<td>A. 4</td>
<td>OE</td>
</tr>
<tr>
<td>A. 5</td>
<td>CE</td>
</tr>
<tr>
<td>A. 6</td>
<td>I/O</td>
</tr>
<tr>
<td>A. 7</td>
<td>I/O</td>
</tr>
<tr>
<td>A. 8</td>
<td>I/O</td>
</tr>
<tr>
<td>A. 9</td>
<td>I/O</td>
</tr>
<tr>
<td>A. 10</td>
<td>I/O</td>
</tr>
<tr>
<td>I/O. 11</td>
<td>I/O</td>
</tr>
<tr>
<td>I/O. 12</td>
<td>I/O</td>
</tr>
<tr>
<td>I/O. 13</td>
<td>I/O</td>
</tr>
<tr>
<td>Vcc</td>
<td>14</td>
</tr>
</tbody>
</table>

■ Operation Mode

<table>
<thead>
<tr>
<th>CE</th>
<th>OE</th>
<th>WE</th>
<th>I/O</th>
<th>MODE</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>Low Z Read</td>
</tr>
<tr>
<td>L</td>
<td>X</td>
<td>L</td>
<td>L</td>
<td>High Z Write</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>High Z Standby</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>X</td>
<td>L</td>
<td>High Z Refresh</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>X</td>
<td>L</td>
<td>High Z</td>
</tr>
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■ Block Diagram
### Description

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Name</th>
<th>I/O</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>CLK</td>
<td>I</td>
<td>Single-phase clock input. When the clock input is set to DC (&quot;1&quot; or &quot;0&quot; level continued), the MPU stops and holds that state.</td>
</tr>
<tr>
<td>2-5</td>
<td>D0-D7</td>
<td>I/O</td>
<td>8-bit bidirectional data bus.</td>
</tr>
<tr>
<td>6</td>
<td>Vcc</td>
<td>–</td>
<td>+5V power supply.</td>
</tr>
<tr>
<td>11/17</td>
<td>NC (PLCC Only)</td>
<td>–</td>
<td>Not connected internally. Set to open.</td>
</tr>
<tr>
<td>12</td>
<td>INT</td>
<td>I</td>
<td>Maskable interrup request signal. Interrupts are given by a peripheral LSI. When the interrupt enable flipflop (IFF) is set to &quot;1&quot; by software, the interrupt is accepted. INT is usually used as the wired OR and a pull-up resistor is added externally.</td>
</tr>
<tr>
<td>13</td>
<td>NMI</td>
<td>I</td>
<td>Non-maskable interrupt request signal. This interrupt request has priority over the maskable interrupt and does not depend on the state of the interrupt enable flipflop (IFF).</td>
</tr>
<tr>
<td>14</td>
<td>HALT</td>
<td>I</td>
<td>Halt signal. &quot;0&quot; is output when the MPU executes a HALT command and is set to the HALT state.</td>
</tr>
<tr>
<td>15</td>
<td>MREQ</td>
<td>I</td>
<td>Memory request signal. &quot;0&quot; is output when there is an effective address for memory access on the address bus. MRFQ also goes &quot;0&quot; together with the RFSH signal during memory refresh.</td>
</tr>
<tr>
<td>Pin No.</td>
<td>Name</td>
<td>I/O</td>
<td>Function</td>
</tr>
<tr>
<td>--------</td>
<td>------</td>
<td>-----</td>
<td>----------</td>
</tr>
<tr>
<td>16</td>
<td>IORQ</td>
<td>O</td>
<td>Input/output request signal. “0” is output when the address for input/output is on the low-order 8 bits (A0-A7) of the address bus when an input or output is given. The IORQ signal is also output together with the MI signal when an interrupt is acknowledged to inform the peripheral LSI that the interrupt response vector can be superimposed on the data bus.</td>
</tr>
<tr>
<td>18</td>
<td>RD</td>
<td>O</td>
<td>READ signal. “0” is output while the MPU can accept the data from a peripheral LSI. The data in the designated LSI or memory is gated by this signal and can be superimposed on the MPU data bus.</td>
</tr>
<tr>
<td>19</td>
<td>WR</td>
<td>O</td>
<td>WRITE signal. This is output when the data to be stored in the memory or peripheral LSI is superimposed on the MPU data bus.</td>
</tr>
<tr>
<td>20</td>
<td>BUSACK</td>
<td>O</td>
<td>Bus acknowledge signal. When the BUSREQ signal is input, the BUSACK signal informs the peripheral LSIs that the address bus and data bus of the MPU and the MREQ, IORQ, RD and WR signals have been set to high impedance.</td>
</tr>
<tr>
<td>21</td>
<td>WAIT</td>
<td>I</td>
<td>WAIT signal. The WAIT signal informs the MPU that the designated memory or peripheral LSI is not ready for data transfer. The MPU continues in the wait state as long as the WAIT signal is “0”.</td>
</tr>
<tr>
<td>22</td>
<td>BUSREQ</td>
<td>I</td>
<td>Bus request signal. The BUSREQ signal requests to set the address bus and data bus of the MPU and the MREQ, IORQ, RD and WR signals to high impedance. BUSREQ is usually used as the wired OR and a pull-up resistor is connected externally.</td>
</tr>
<tr>
<td>23</td>
<td>RESET</td>
<td>I</td>
<td>Reset signal. The RESET signal initializes the MPU and should be active (“0”) for at least 3 clock-signal periods.</td>
</tr>
<tr>
<td>24</td>
<td>M1</td>
<td>O</td>
<td>Signal that indicates machine cycle 1. “0” is output together with the MREQ in the command operation code fetch cycle. When 2-byte operation codes are executed, M1 is output each time the operation code is fetched. M1 is output with the IORQ signal in the maskable interrupt acknowledge cycle.</td>
</tr>
<tr>
<td>25</td>
<td>RFSH</td>
<td>O</td>
<td>Refresh signal. “0” is output when the address that refreshes the dynamic memory is on the low-order 7 bits of the address bus. The MREQ signal also goes active (“0”) in this state.</td>
</tr>
<tr>
<td>26</td>
<td>Vss</td>
<td>–</td>
<td>0V power supply</td>
</tr>
<tr>
<td>27-32</td>
<td></td>
<td></td>
<td>16-bit address bus.</td>
</tr>
<tr>
<td>34-38</td>
<td>A0-A15</td>
<td>O</td>
<td>Address the memory and input/output ports. The address for refreshing is output during refreshing.</td>
</tr>
</tbody>
</table>
IC5
IC UPD4364G-15L
Parts No.: 315-0546-A
IC MB8464A-80
Parts No.: 315-0651-A
IC LC3564PM-10L
Parts No.: 315-0753-10A
IC KM6264BLG-10
Parts No.: 315-0754-A
IC LC3664BML-85H
Parts No.: 315-0766-85
IC CXK5864CM-70LL-T6
Parts No.: 315-0773-A

![Outside View](image)

IC MB8464A-10LL
Parts No.: 315-0635-A
IC LC3564PM-12L
Parts No.: 315-0753-12A
IC KM6264BLG-10
Parts No.: 315-0754-A
IC LC3664BML-10H
Parts No.: 315-0766-10

### Pin Layout

<table>
<thead>
<tr>
<th>NC</th>
<th>28</th>
<th>27</th>
<th>WC</th>
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</thead>
<tbody>
<tr>
<td>26</td>
<td>WE</td>
<td>25</td>
<td>CE</td>
</tr>
<tr>
<td>24</td>
<td>OE</td>
<td>23</td>
<td>A</td>
</tr>
<tr>
<td>22</td>
<td>A</td>
<td>21</td>
<td>A</td>
</tr>
<tr>
<td>20</td>
<td>A</td>
<td>19</td>
<td>CE</td>
</tr>
<tr>
<td>18</td>
<td>CE</td>
<td>17</td>
<td>GND</td>
</tr>
<tr>
<td>16</td>
<td>IO</td>
<td>15</td>
<td>IO</td>
</tr>
<tr>
<td>14</td>
<td>IO</td>
<td>13</td>
<td>IO</td>
</tr>
</tbody>
</table>

- A₁–A₉: ADDRESS INPUT
- CE, CE₂: CHIP ENABLE 1, 2
- OE: OUTPUT ENABLE INPUT
- I/O, I/O: DATA IN/OUTPUT
- Vᵣ: +5V POWER SUPPLY
- GND: GROUND
- WE: WRITE ENABLE INPUT
- NC: NO CONNECTION

### Operation Mode

<table>
<thead>
<tr>
<th>CE₁</th>
<th>CE₂</th>
<th>OE</th>
<th>WE</th>
<th>MODE</th>
<th>OUTPUT STATE</th>
<th>POWER SUPPLY CURRENT</th>
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</thead>
<tbody>
<tr>
<td>H</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>Non-Select</td>
<td>High Impedance</td>
<td>Iₑₑ</td>
</tr>
<tr>
<td>X</td>
<td>L</td>
<td>X</td>
<td>X</td>
<td>(Power Down)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>Output Disable</td>
<td></td>
<td></td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>Read</td>
<td>Dₜₒᵤₜ</td>
<td>Iₒₒₙ</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>X</td>
<td>L</td>
<td>Write</td>
<td>Dᵢₚ</td>
<td>Iₒₒₙ</td>
</tr>
</tbody>
</table>

### Block Diagram

- ADDRESS BUFFER
- ROW DECODER
- 65,536 BIT (256 x 256) MEMORY CELL ARRAY
- INPUT DATA CONTROL
- SENSE SWITCH
- COLUMN DECODER
- ADDRESS BUFFER
- OUTPUT CONTROL
<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Name</th>
<th>I/O</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SD0</td>
<td>I</td>
<td>Dual Port RAM Interface Signals.</td>
</tr>
<tr>
<td>2</td>
<td>SD1</td>
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<td></td>
</tr>
<tr>
<td>3</td>
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<tr>
<td>9</td>
<td>- SE1</td>
<td>O</td>
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<tr>
<td>10</td>
<td>- SE0</td>
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<tr>
<td>11</td>
<td>- SC</td>
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<tr>
<td>12</td>
<td>- RAS1</td>
<td>I/O</td>
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<td>- CAS1</td>
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<tr>
<td>14</td>
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<tr>
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<tr>
<td>17</td>
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<td>I/O</td>
<td>Dual Port RAM Interface Signals.</td>
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<td>RD1</td>
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<tr>
<td>19</td>
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<td>RD3</td>
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<tr>
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<td>VSS</td>
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<td>GND</td>
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<td>RD4</td>
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<td>RD5</td>
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<td>Dual Port RAM Interface Signals.</td>
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<td>AD3</td>
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<tr>
<td>33</td>
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</tr>
<tr>
<td>34</td>
<td>VIDEO AVSS</td>
<td>-</td>
<td>VIDEO+PSG</td>
</tr>
<tr>
<td>35</td>
<td>R (ANLONG)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>36</td>
<td>G (ANLONG)</td>
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<tr>
<td>37</td>
<td>B (ANLONG)</td>
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<tr>
<td>38</td>
<td>VIDEO AVDD</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>39</td>
<td>- YS</td>
<td>O</td>
<td></td>
</tr>
<tr>
<td>40</td>
<td>SPA/B</td>
<td>I/O</td>
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</table>

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Name</th>
<th>I/O</th>
<th>Function</th>
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<tbody>
<tr>
<td>41</td>
<td>- VSYNC</td>
<td>O</td>
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</tr>
<tr>
<td>42</td>
<td>- CSYNC</td>
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<td>VIDEO+PSG</td>
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<tr>
<td>43</td>
<td>- HSYNC</td>
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<tr>
<td>44</td>
<td>VDD</td>
<td>-</td>
<td>Power Supply.</td>
</tr>
<tr>
<td>45</td>
<td>- M3</td>
<td>I</td>
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</tr>
<tr>
<td>46</td>
<td>- NTSC</td>
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<td>- VPA</td>
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<tr>
<td>48</td>
<td>- HALT</td>
<td>O</td>
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</tr>
<tr>
<td>49</td>
<td>- RESET</td>
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<td>68000 Interface Signals.</td>
</tr>
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<td>FC0</td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>51</td>
<td>FC1</td>
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<tr>
<td>52</td>
<td>- MREQ</td>
<td>I/O</td>
<td>Z80 Interface Signals.</td>
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<td>VSS</td>
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<td>AUSS</td>
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<td>55</td>
<td>MOR (ANLONG)</td>
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<td>FM</td>
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<td>56</td>
<td>MOL (ANLONG)</td>
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<td>57</td>
<td>SOUND AVDD</td>
<td>-</td>
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<tr>
<td>58</td>
<td>- SOUND</td>
<td>I/O</td>
<td>Use This Pin Set To Open Certainly.</td>
</tr>
<tr>
<td>59</td>
<td>- ZRES</td>
<td>I/O</td>
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<td>60</td>
<td>- ZBAK</td>
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</tr>
<tr>
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<td>- NMI</td>
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<td>Z80 Interface Signals.</td>
</tr>
<tr>
<td>62</td>
<td>- ZBR</td>
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<td>- WAIT</td>
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<tr>
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<td>- EOE</td>
<td>O</td>
<td>P-SRAM Interface.</td>
</tr>
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<td>67</td>
<td>- REF</td>
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<tr>
<td>68</td>
<td>- CAS2</td>
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<td>- RAS2</td>
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<td>- CEO</td>
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<td>I/O</td>
<td>Function</td>
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<tr>
<td>80</td>
<td>VDD</td>
<td>-</td>
<td>Power Supply.</td>
</tr>
<tr>
<td>81</td>
<td>TEST0</td>
<td>I/O</td>
<td>Test Signal. (Set To &quot;0&quot; Certainly.)</td>
</tr>
<tr>
<td>82</td>
<td>TEST1</td>
<td>I</td>
<td>Test Signals. (These Pins Set To All Open.)</td>
</tr>
<tr>
<td>83</td>
<td>TEST2</td>
<td>I/O</td>
<td>Joy Pad Interface.</td>
</tr>
<tr>
<td>84</td>
<td>TEST3</td>
<td>I</td>
<td>Joy Pad Interface.</td>
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Parts No.: 315-0423
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Outside View

Block Diagram

Pin Layout
IC BA10324AF-T1
Parts No.: 313-5221-A

IC LM324
Parts No.: 313-5063-A

- Outside View

- Pin Layout
### 8-1. EXPLODED VIEW

![EXPLODED VIEW Diagram]

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PAL, RGB → MEGA DRIVE II
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8-4. ACCESSORIES/PACKAGE LIST

For GENESIS II

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