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AICA (FQ8005)
Sound-block User's Manual
Ver. 1.00

Contents

Overview of Technology

Electrical Specifications

History of Updates

Contents

Overview of AICA

Internal CPU (ARM7).

- Readied with seven prioritized interrupt flags (registers).

PCM Sound block.

- The PCM data is 16- or 8-bit linear format.
- The ADPCM data is 4-bit yamaha original format.
- Independent LFO mounted in separate slots.
- 64-ch,four-segment EG.
- Forward loop function.
- Generation of up to 64 sounds.
- LPF for time transition of cutoff frequency through four-segment EG.
- ADPCM also capable of pitch change (1 octave maximum).

128-step DSP

- DSP that tuned up SCSP.

Digital mixer

By connecting external 16M bit SDRAM, the CPU, sound block, DSP and G2 i/F block can be used together.

Supports RTC(real time clock) back up_able by externally adding battery.

Contents

Pin Table

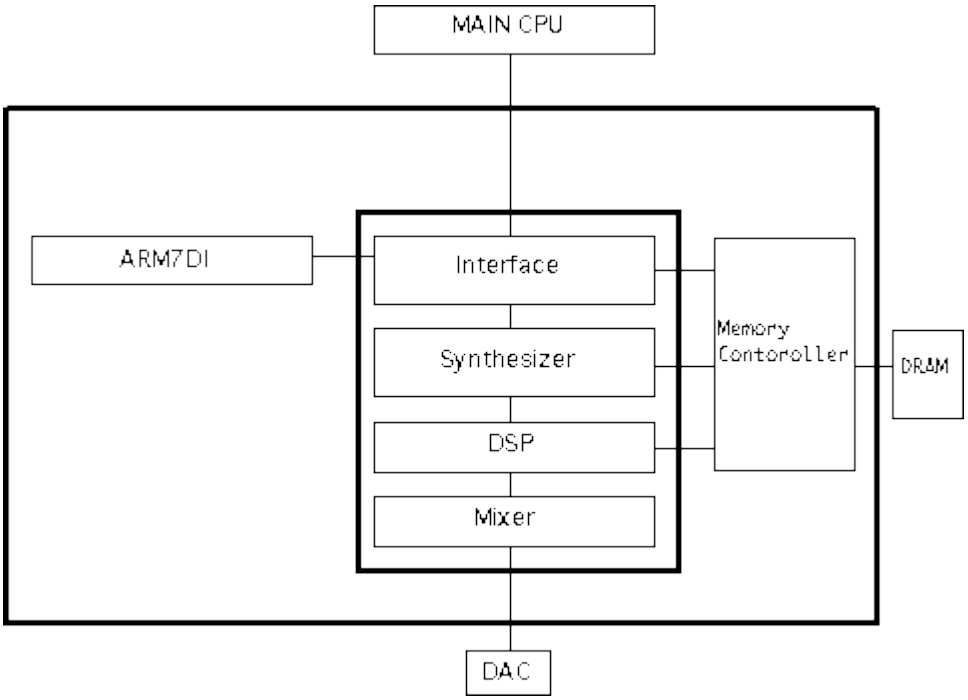
Signal Name	Pin	Function Overview	
CK33 FLC VDDP VSSP	1 1 1 1	Master clock (33 MHz) Filter capacity for PLL Power source for PLL GND for PLL	
VRTC RTCK	1 2	Power source for RTC RTC clock (32 k)	
RESETN	1	Reset signal	3.3 V TTL
INTN	1	External interrupt request input	3.3V TTL
ESD EBCK ELRCK	1 1 1	DIGITAL AUDIO I/F serial data input DIGITAL AUDIO I/F BCK DIGITAL AUDIO I/F LRCK	3.3V TTL 3.3V TTL 3.3V TTL
MIDIIN MIDIOUT	1 1	MIDI input MIDI output	3.3V TTL 3.3V TTL
MCCK MCA[15:0]	1 16	G1 bus clock (98.4 M/4) Main CPU address data bus	3.3V TTL 3.3V TTL

MCFRAMEN MCBHEN MCBLEN MCRDYN MCDSN MCTREQN MCINTN	1 1 1 1 1 1 1	Main CPU #FRAME signal Main CPU #BHE signal Main CPU #BLE signal Main CPU #RDY signal Main CPU #DS signal Main CPU #TREQ signal Main CPU #INT signal	3.3V TTL 3.3V TTL 3.3V TTL 3.3V TTL 3.3V TTL 3.3V TTL
DSD DSCK DBCK DLRCK	1 1 1 1	DAC I/F serial data output DAC I/F system clock 256 fs DAC I/F BCK DAC I/F LRCK	3.3V TTL 3.3V TTL 3.3V TTL 3.3V TTL
MRASN[MWEN] MWEN[MCASLN] MCASN[MEASON] MCSN MCLK MLDQM MHDQM MA[12:0] MD[15:0]	1 1 1 1 1 1 1 13 16	Sound memory RAS signal Sound memory WE signal Sound memory CAS signal Sound memory CS signal CLK signal for sound memory LDQM signal for sound memory HDQM signal for sound memory Sound memory address Sound memory data	3.3V TTL 3.3V TTL 3.3V TTL 3.3V TTL 3.3V TTL 3.3V TTL 3.3V TTL 3.3V TTL 3.3V TTL
VDD VSS	- -	Power source 3.3 V GND	
NTRST TCK TDI TDO TMS	1 1 1 1 1	Pins for embedded ICE	3.3V TTL 3.3V TTL 3.3V TTL 3.3V TTL 3.3V TTL
TEST[1:0]	2	Pins for testing	
Total	85	(128QFP)	

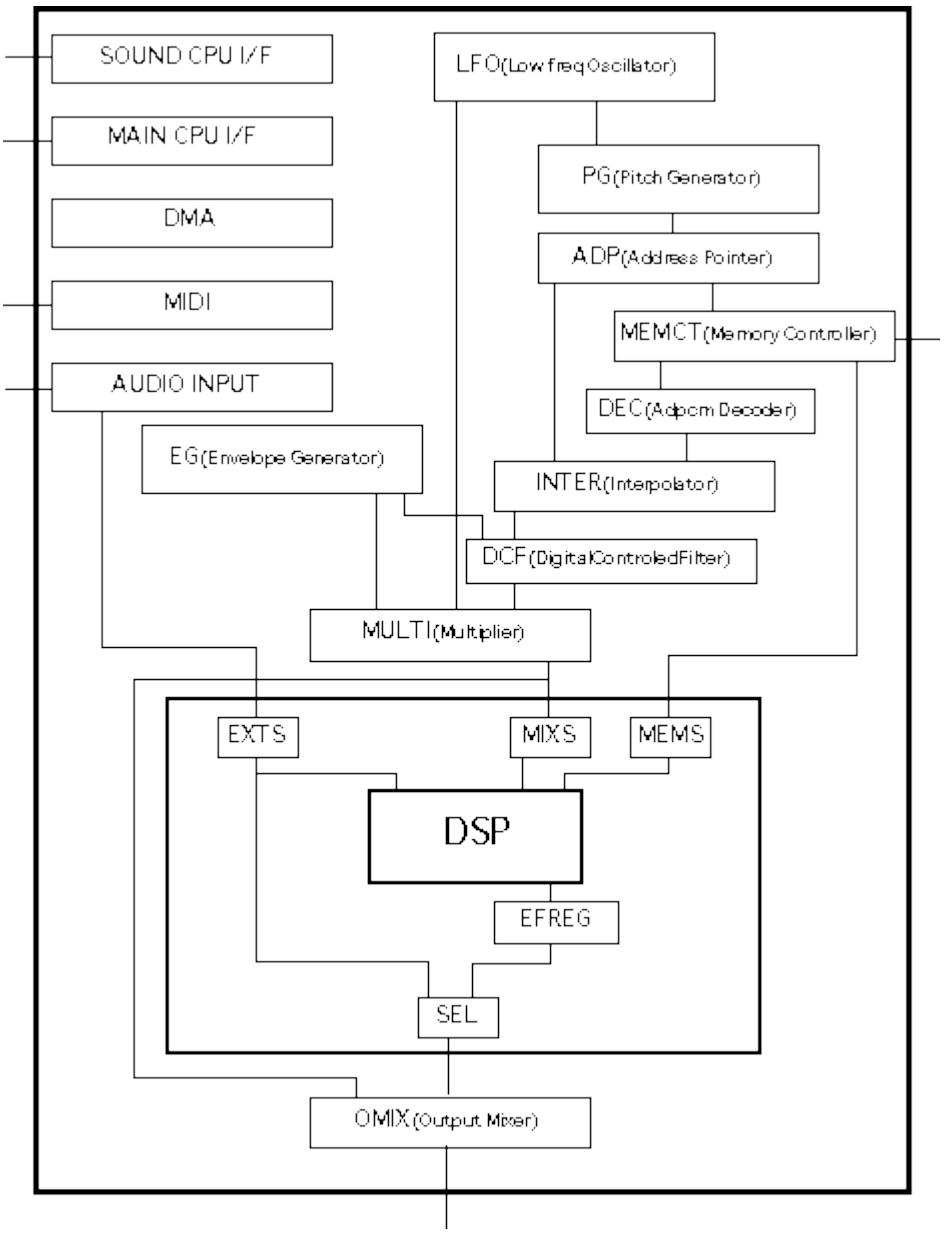
Contents

Block diagram

Memory controller



Sound block diagram



DCF (Digital Controlled Filter)

Contents

Register map

ADDRESS	AREA
00000000～007FFFFF	DRAM_AREA*
00800000～008027FF	CHANNEL_DATA
00802800～00802FFF	COMMON_DATA
00803000～00807FFF	DSP_DATA

Note:

Space that DRAM can use depends on on-board memory size.

Channel data

Asterisks indicate changes after MIG.

ADDRESS	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
00800000	KX	KB	--			SS*	LP*	PCMS*	SA[22:16]*								KX:KYONEX
00800004	SA[15:0]*																LP:LPCTL
00800008	LSA[15:0]																KB:KYONB
0080000C	LEA[15:0]																SS:SSCTL
00800010	D2R[4:0]					D1R[4:0]				--	AR[4:0]						
00800014	--	LS	KRS[3:0]			DL[4:0]				RR[4:0]							LS:LPSLNK
00800018	--	OCT[3:0]*		--	FNS[9:0]												
0080001C	RE	LFOF[4:0]				PLFOWS	PLFOS[2:0]		ALFOWS	ALFOS[2:0]							RE:LFORE
00800020	--	TL[7:0]								ISEL[3:0]			--				
00800024	IMXL[3:0]			DISDL[3:0]				--	DIPAN[4:0]								
00800028	--								Q[4:0]*								
0080002C	--		FLV0[12:0]*														
00800030	--		FLV1[12:0]*														
00800034	--		FLV2[12:0]*														
00800038	--		FLV3[12:0]*														
0080003C	--		FLV4[12:0]*														
00800040	--		FAR[4:0]				--	FD1R[4:0]									
00800044	--		FD2R[4:0]				--	FRR[4:0]									
00800080 | 008000C4	SLOT 1 CONTROL REGISTER																
00801F80 | 00801FC4	SLOT 63 CONTROL REGISTER																
00802000	--		EFSDL[3:0]				--	EFPAN[4:0]									DSP_OUT_1
00802044	--		EFSDL[3:0]				--	EFPAN[4:0]									DSP_OUT_18

Common data (not affected by channel)

Asterisks indicate changes after MIG.

ADDRESS	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
00802800	MN	--					M8	D8	VER[3:0]				MVOL[3:0]				D8:DAC18B M1:MEM8MB
00802804	$T	RBL		--	RBP[22:11]*												$T:TESTB0 (IC TEST)
00802808	--			OF	OE	IO	IF	--	MIBUF[7:0]								IF:MIFUL IO:MIOVF
0080280C	--	AF	MSLC[5:0]*						MOBUF[7:0]								OE:MOEMP OF:MOFUL AF:AFSET
00802810	LP*	SGC	EG[12:0]*														MN:Mono

00802814	CA[15:0]*																	
00802880	DMEA[22:16]							--	$TSCD[2:0]			$T	MRWINH[3:0]					$＊＊＊ (IC TEST)
00802884	DMEA[15:1]																--	
00802888	GA	DRGA[14:1]															--	
0080288C	DI	DLG[14:1]															EX	GA:DGATE DI:DDIR EX:DEXE
00802890	--					TACTL[2:0]			TIMA[7:0]									
00802894	--					TBCTL[2:0]			TIMB[7:0]									
00802898	--					TCCTL[2:0]			TIMC[7:0]									
0080289C	--					SCIEB[10:0]												
008028A0	--					SCIPD[10:0]												
008028A4	--					SCIRE[10:0]												
008028A8	--								SCILV0[7:0]									
008028AC	--								SCILV1[7:0]									
008028B0	--								SCILV2[7:0]									
008028B4	--					MCIEB[10:0]												
008028B8	--					MCIPD[10:0]												
008028BC	--					MCIRE[10:0]												
00802C00	--																AR	AR:ARMRST
00802D00	--											L7	L6	L5	L4	L3	L2	L1	L0	割り込み用 RP:ReadProtection
00802D04	--										RP	M7	M6	M5	M4	M3	M2	M1	M0	割り込み用
00802E00	RTC[31:16]*																	
00802E04	RTC[15:0]*																	

DSP data

Asterisks indicate changes after MIG.

ADDRESS	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
00803000 ｜ 008031FF	COEF REG "COEF[12:0]"													00	00	00	00～127
00803200 ｜ 008032FF	MEMORY ADDRESS REG "MADRS[16:1]"																00～63
00803400	DSP MICRO PROGRAM "MPRO[63:48]"																STEP_0
00803404	DSP MICROPROGRAM "MPRO[47:32]"																
00803408	DSP MICROPROGRAM "MPRO[31:16]"																
0080340C	DSP MICROPROGRAM "MPRO[15:0]"																
00803410 ｜	｜																STEP_1～STEP_126

| 00803BEC			
00803BF0	DSP MICRO PROGRAM "MPRO[63:48]"		STEP_127
00803BF4	DSP MICROPROGRAM "MPRO[47:32]"		
00803BF8	DSP MICROPROGRAM "MPRO[31:16]"		
00803BFC	DSP MICROPROGRAM "MPRO[15:0]"		
00804000	--	LOW "TEMP[7:0]"	00～127
| 008043FF	TEMPBUFFER HIGH "TEMP[23:8]"		
00804400	--	LOW "MEMS[7:0]"	00～31
| 008044FF	SOUND MEMORY DATA HIGH "MEMS[23:8]"		
00804500	--	"MIXS[3:0]"	00～15
| 0080457F	MIXSOUND SLOT DATA STACK "MIXS[19:4]"		
00804580 | 008045BF	EFCTED DATA OUTPUT "EFREG[15:0]"		00～15
008045C0 | 008045C7	EXTERNAL INPUT DATA STACK "EXTS"		00～01

Contents

Overview of Registers

Channel data

KYONEX

All slots are made KEY_ON or OFF when "1" is written. Writing"0" has no effect.

KYONB

Registers KEY_ON or OFF.
(To simultaneously make KEY_ON, set this bit to "1" for all slots to be made ON, and write "1" to KEYONEX of any of those slots.

SSCTL

- 0: Uses local SDRAM data as sound input data.
- 1: Uses noise as sound input data.

LPCTL

- 0: Loop OFF
  (LSA and LEA settings are necessary, so processing ends when LEA is reached.)
- 1: Forward loop

PCMS[1:0]

- 0: 16-bit PCM (2's complement format)
- 1: 8-bit PCM (2's complement format)
- 2: 4-bit ADPCM (Yamaha format)
- 3: Use prohibited

SA [22:0]

Start address of sound data specified with byte address.
However, when PCMS = 0, SA0 (LSB of SA [22:0]) has to be "0". @

LSA [15:0]

Loop start address of sound data specified with sample count from SA(Start Address).

- 1: Sample frequency is byte count for PCM8B = 1, word (16-bit) count for PCM8B = 0, and 1/2 byte count for ADPCM.
- 2: Minimum value that can be set is restricted by the pitch and loop mode.

LEA [15:0]

Loop end address of sound data specified with sample count from SA.

- 1: Maximum value that can be set is restricted by the pitch and loop mode.
- 2: To enable interpolation, setting of LEA = FFFF[X] is prohibited.
- 3: SA * LSA regardless of loop mode.

Notes on loop

AR [4:0]

Specifies the rate of transition of EG in attack status. (Volume transition is increased.)

DIR [4:0]

Specifies the rate of transition of EG in decay 1 status. (Volume transition is decreased.)

D2R [4:0]

Specifies the rate of transition of EG in decay 2 status. (Volume transition is decreased.)

RR [4:0]

Specifies the rate of transition of EG in release status. (Volume transition is decreased.)

DL [4:0]

Specify the EG level for the transition from decay 1 to decay 2.

KRS [3:0]

Specifies the rate of the EG key rate scaling. (Integer)

```
0 [X] = Minimum scaling
        :
        :
E [X] = Maximum scaling
F [X] = Scaling OFF
```

LPSLNK

Loop start link function: EG shifts to decay 1 when the address of the read sound_slot_input_data exceeds the loop start address.
(When EG = "000", there is no transition.) For this case, there may not be a transition to decay 2, depending on the setting of DL register.

Notes on EG

OCT [3:0]

Specifies octave as two's complement.
Values in parentheses are +1 octave for ADPCM.

OCT	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
Tone	-8	-7	-6	-5	-4	-3	-2	-1	0	+1	(+2)	(+3)	(+4)	(+5)	(+6)	(+7)

FNS [9:0]

Specifies sound pitch setting to FNS and OCT register.

```
Pitch: P [CENT} = 1200 x LOG 2 ((210 + FNS)/210)
```

For FNS = 0 (and OCT = 0), the tone matches the sampling source.
Also, the pitch difference (pitch precision) equivalent to the LSB of FNS is 1.69 centimeters.

Notes on PG

LFORE

Specifies whether or not to initialize LFO.
(Setting has no effect if noise has been selected.)

- 1: Resets LFO.
- 0: Does not reset LFO.

LFOF [4:0]

Specifies the oscillation frequency of LFO.
(Setting has no effect if noise has been selected.)

ALFOWS [1: 0]

Specifies the shape of the ALFO waveform.

PLFOWS [1: 0]

Specifies the shape of the PLFO waveform.

ALFOS [2:0]

Specifies the extent of mixing to the EG of LFO.

PLFOS [2:0]

Specifies the extent of the effect on the pitch of LFO.

Notes on LFO

ISEL [3:0]

Specifies the mix register address for each slot when sound slot output data is input to the DSP's mix register (MIXS).

Note:
MIXS is the input for DSP to obtain the sum of the input for all slots.

- MIXS has an area for adding per slot, and an area for keeping the interval of one sample; these areas can be allocated alternately. Hence, reading by the DSP side can be done at any step.
- Input to MIXS must be set so that the sum does not overflow 0 dB. (There is no overflow protect function.)

TL [7:0]

Total level: The actual amount of attenuation is specified by placing this value in the EG value.

DIPAN [4:0]

Specifies the position for each slot when direct data is sent.

EFPAN [4:0]

Specifies the position for each slot for effect data and external input data.

IMXL [3:0]

Specifies the level for each slot when sound slot output data is input to the DSP mix register (MIXS).

DISDL [3:0]

Specifies the send level for each slot when direct data is output to DAC.

EFSDL [3:0]

Specifies the send level when effect data and external input data is sent to DAC. The send level is specified for each slot. (Codes are the same as for DISDL.)

Register	Volume
0	-MAXdB
1	-42dB
2	-39dB
|	|
D	-6dB
E	-3dB
F	0dB

Notes on mixer

Q [4:0]

Resonance data

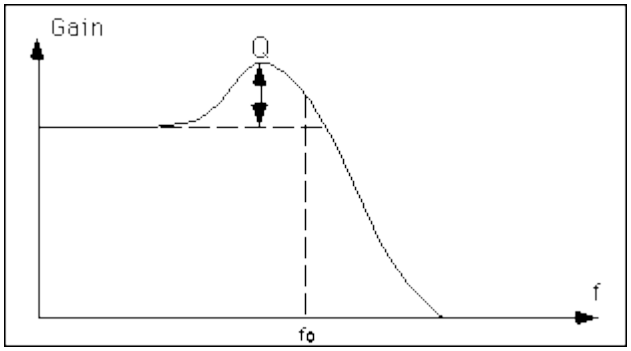
Sets Q for the FEG filter. Values from -3.00 through 20.25 dB can be set. The relationships between bits and gain are as follows:

```
Q [dB] = 0.75 x register value -3
```

Example of setting

DATA	GAIN[dB]	DATA	GAIN[dB]
11111	20.25	00100	0.00
11100	18.00	00011	-0.75
11000	15.00	00010	-1.50
10000	9.00	00001	-2.25
01100	6.00	00000	-3.00
01000	3.00		
00110	1.50		

The following figure defines Q.



FLV0 [12:0]

Cutoff frequency at the time of attack start

FLV1 [12:0]

Cutoff frequency at the time of attack end (dacay start time)

FLV2 [12:0]

Cutoff frequency at the time of decay end (sustain start time)

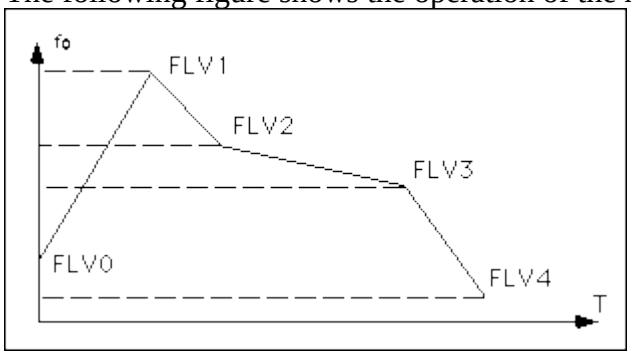
FLV3 [12:0]

Cutoff frequency at the time of KOFF

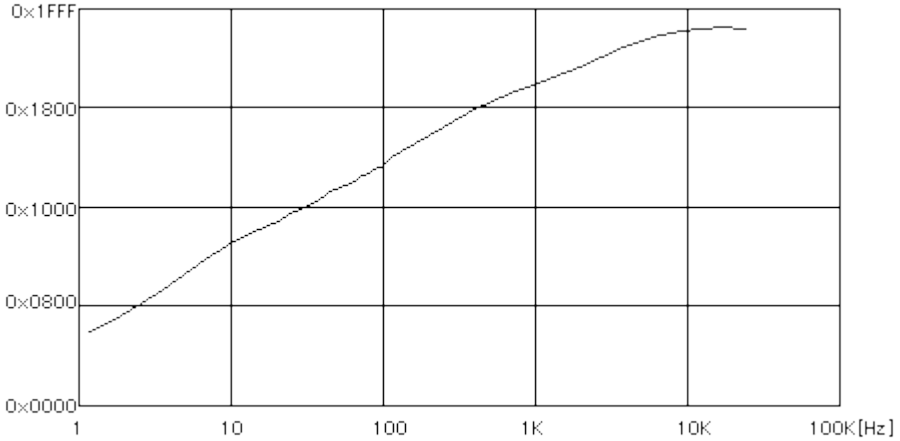
FLV4 [12:0]

Cutoff frequency after release

The following figure shows the operation of the registers.



Correspondence between filter cutoff frequencies and registers is roughly as below.



* When filter is through, Q is 4H and FLV* is 1FFFH.

FAR [4:0]

Specifies the rate of transition of FEG in attack status. (Volume transition is increased.)

FD1R [4:0]
Specifies the rate of transition of FEG in decay 1 status. (Volume transition is decreased.)

FD2R [4:0]
Specifies the rate of transition of FEG in decay 2 status. (Volume transition is decreased.)

FRR [4:0]
Specifies the rate of transition of FEG in release status. (Volume transition is decreased.)

Common data

MONO
- 1: Makes panpot?? information invalid.
- 0: Makes panpot information valid.

Note:
When panpot information has been made invalid, the sound coming from the channel on one side will double in volume, so the setting of MVOL must be lowered.

MVOL [3:0]
Master volume for digital output to DAC

Mixer notes

DAC18B
- 1: The digital output is the 18-bit DAC interface.
- 0: The digital output is the 16-bit DAC interface.

MEM8MB
Specifies the memory to be used.
- 0: 16M_DRAM
- 1: 64M_DRAM

Relationships between sound memory space and used memory

VER [3:0]
Reads out the LSI version based on this manual.

RBL [1:0]
Specifies the length of the ring buffer.
- 0: 8 K words
- 1: 16 K words
- 2: 32 K words
- 3: 64 K words

RBP [22:11]
Specifies the leading address of the ring buffer. (1 K word limit)

MIBUF [7:0]
MIDI input data buffer. (Consists of four-byte FIFO.)

MIOVF

Indicates that the input FIFO has overflowed.

MIFUL

Indicates that the input FIFO is full.
(The above two flags show the status before MIBUF [7:0] is read.)

MOFUL

Indicates that the output FIFO is full.

MOEMP

Indicates that the output FIFO is empty.

MOBUF [7:0]

MIDI output data buffer

AFSEL

Decides whether to make the EG monitor AEG or FEG.

- 0: AEG monitor
- 1: FEG monitor

MSLC [5:0]

Specifies the slot number to monitor SGC, CA, EG, and LP.

SGC [1:0]

Monitors the status of the current EG.

- 0: Attack
- 1: Decay 1
- 2: Decay 2
- 3: Release

CA [15:10]

Currently, shows the sample position read from the sound source as the 16 high-order bits of the relative sample No. from SA. The lowest order bit is equivalent to one sample.

EG [12:0]

Monitors the 13 high-order bits of the current EG value. During AEG monitoring, the low-order three bits are always "0".

LP

Loop end flag
The channel is selected by MSLC [5:0]. This flag shows that the loop has ended.
This flag is cleared to "0" when it is read.

MRWINH [3:0]

Writing "1" to this flag prohibits reading for the corresponding sound memory access. (Register access cannot be prohibited.)

- Bit 0: Access by DSP
- Bit 1: Read by sound source
- Bit 2: Access by SCPU
  (Reading by SCPU prohibited because cancel cannot be done from SCPU.)
- Bit 3: Access by MCPU

DGATE

Specifies to clear the DMA transmission destination field to "0".

- 0: Does not clear to "0".
- 1: Clears to "0".

DDIR

Specifies the direction for DMA transmission.

- 0: Transmits from sound memory to SCSP register.
- 1: Transmits from SCSP register to sound memory.

DEXE

Specifies the start of DMA. (Cleared to "0" when DMA ends.)

- DMA starts when "1" is written.
- Writing "0" has no effect.

DMEA [22:1]

The word address specifies the sound memory address that starts DMA.

DRGA [14:1]

The word address specifies the internal register address that starts DMA.

DLG [14:1]

Specifies the DMA transmission word count.

Caution:

Fields of the source and destination must not exceed the memory fields or internal register fields.
During DMA transmission, registers associated with DMA must not be changed.

Notes:

Registers are assigned to the memory 100000-100EE3.
The transmission address always changes in the increasing direction.

TACTL [2:0]

Specifies the increment cycle of timer A.

- 0: One increment per sample.
- 1: One increment per two samples.
- 2: One increment per four samples.
- 3: One increment per eight samples.
- 4: One increment per 16 samples.
- 5: One increment per 32 samples.
- 6: One increment per 64 samples.
- 7: One increment per 128 samples.

TIMA [7:0]

Timer A (Generates an interrupt request at the timing when the UP counter changes from all "1" to all "0".)

TBCTL [2:0]

Specifies the increment cycle for timer B. (The code is the same as for timer A.)

TIMB [7:0]

Timer B (Generation of interrupt is the same as for timer A.)

TCCTL [2:0]

Specifies the increment cycle for timer C. (The code is the same as for timer A.)

TIMC [7:0]

Timer C (Generation of interrupt is the same as for timer A.)

SCIPD [10:0]

Holds the SCPU interrupt request. (Bit correspondence is as below.)

- Bit 0 (R): Requests interrupt to external interrupt input pin "INTON". (SCSI)
- Bit 1 (R): Reserved.
- Bit 2 (R): Reserved.
- Bit 3 (R): MIDI input interrupt.
  (Interrupt request generated when input FIFO has fetched valid data. Hence, if the CPU reads FIFO data, it must read the lot once and leave the FIFO empty. When the FIFO has changed to empty status, the interrupt request is canceled automatically.)
- Bit 4 (R): DMA end interrupt
- Bit 5 (R/W): SCPU interrupt caused by data being written to the CPU, so only "1" can be written. (Writing "0" has no effect.) This flag can be set from either the MCPU or the SCPU.
- Bit 6 (R): Timer A interrupt
- Bit 7 (R): Timer B interrupt
- Bit 8 (R): Timer C interrupt
- Bit 9 (R): MIDI output interrupt.
  (If the output FIFO changes to empty status, an interrupt request is generated.)
  (If the status is no longer empty because data is written to the output FIFO, the interrupt request is canceled automatically.)
- Bit 10 (R): Interrupt of one sample interval

SCIEB [10:0]

Permits an interrupt for the bit corresponding to "1" for the SCPU interrupt permission register.

SCIRE [10:0]

Resets the interrupt request corresponding to the bit written with "1".

SCILV0 [7:0]

Specifies bit 0 of the SCPU interrupt level code defined by the bit correspondence.

SCILV1 [7:0]

Specifies bit 1 of the SCPU interrupt level code defined by the bit correspondence.

SCILV2 [7:0]

Specifies bit 2 of the SCPU interrupt level code defined by the bit correspondence.
(See SCIPD for bit correspondence.)

Notes:

Bit 7 can be used to make one specification for the level of the interrupt request bits 7, 8, 9, and 10.

For the interrupt level by INTON, SCILV2 [0], SCILV1 [0], and SCILV0 [0] correspond to pins SCIPL2N, SCIPL1N, AND SCIPL0N.

MCIPD [10:0]

Holds the MCPU interrupt request.

- Bit 0 (R): Interrupt to external interrupt input pin "INTON". (SCSI)
- Bit 1 (R): Reserved.
- Bit 2 (R): Reserved.
- Bit 3 (R): MIDI input interrupt.
  (Interrupt request generated when input FIFO has fetched valid data. Hence, if the CPU reads FIFO data, it must read the lot once and leave the FIFO empty. When the FIFO has changed to empty status, the interrupt request is canceled automatically.)
- Bit 4 (R): DMA end interrupt
- Bit 5 (R/W): MCPU interrupt caused by data being written to the CPU, so only "1" can be written. (Writing "0" has no effect.)
  This flag can be set from either the MCPU or the SCPU.
- Bit 6 (R): Timer A interrupt
- Bit 7 (R): Timer B interrupt
- Bit 8 (R): Timer C interrupt
- Bit 9 (R): MIDI output interrupt.
  (If the output FIFO changes to empty status, an interrupt request is generated.)
  (If the status is no longer empty because data is written to the output FIFO, the interrupt request is canceled automatically.)
- Bit 10 (R): Interrupt of one sample interval

MCIEB [10:0]

Permits an interrupt for the bit corresponding to "1" for the MCPU interrupt permission register.

MCIRE [10:0]

Resets the interrupt request corresponding to the bit written with "1".

Note:
When the above interrupt request starts, the MCPU interrupt signal MCINTN generates a negative pulse corresponding to one clock of MCCK.
The interrupt level cannot be specified for the MCPU interrupt.

ARMRST

Resets ARM7DI.

- 0: Reset.
- 1: Reset canceled.

Note:
This register can be controlled from the main CPU only.

RP

Sets the DRAM control from the main CPU to the read only status for reading DRAM data.

- 0: Main CPU can read and write DRAM.
- 1: Main CPU can read DRAM.

Note:
This register can perform control from the ARM7DI side only.

L [7:0]

Indicates the No. of the interrupt arriving at ARM7DI. Here, L [7:3] must be used.

Note:
This register can perform control from the ARM7DI side only.

M [7:0]

Sets this bit to "1" when ARM7DI completes interrupt processing, so as to notify interrupt end to the AICA sound block. Here, M [7:1] must be used.

Note:
This register can perform control from the ARM7DI side only.

RTC [31:0] (R/W)

Indicates the status of the counter that increments by 1 every second. Can count approximately 136 years with 32 bits.

DSP data

COEF [12:0]

Buffer for the DSP data quantity. (Data quantity: 128)

Caution:
If the conventional data width of 16 bits is expanded, write "0" to the three undefined lower-order bits of the register map so as to maintain compatibility.

MADRS [16:1]

Buffer for DSP addresses. (Data quantity: 64)

MPRO [63:0]

Buffer for DSP microprograms. (Data quantity: 128)

TEMP [23:0]

DSP work buffer. (Data quantity: 128)
Configured as a ring buffer. The pointer decrements by 1 for each sample.

MEMS [23:0]

Input-data-buffer from wave-memory (Data quantity: 32)
The actual write to MEMS [7:0] is executed at the same time as the write to MEMS [23:16].

MIXS [19:0]

Buffer for sound data from input mixer. (Data quantity: 16)

Caution:
Writing to MIXS [19:0] is used for LSI tests. Writing other than in test mode is invalid for the following reasons:

- Regardless of the setting, data is constantly being written from the sound block.
- A second generation's worth of data is held for adding all slots, but the generation cannot be specified at access.

EFREG [15:0]

DSP output buffer. (Data quantity: 16)

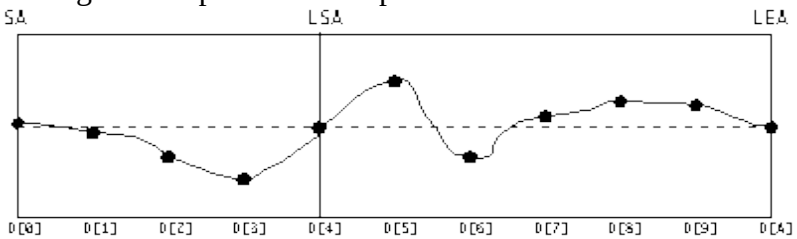
EXTS [15:0]

Data buffer for digital audio input. (Data quantity: 4)

Overview of Technology

Loop Control

Settings for loop data and loop-associated addresses are as below.



Settings for the above data are "3" for LSA and "A" for LEA.

Further, when SA is 100h, the sound memory is allocated as below.
(Little-endian)

When PCMS = 2 (ADPCM)				
	15-12	15-8	7-4	3-0
100	D3	D2	D1	D0
102	D7	D6	D5	D4
104	--	DA	D9	D8

When PCMS = 1		
	15-8	7-0
100	D1	D0
102	D3	D2
:		
108	D9	D8
10A	--	DA

When PCMS = 0	
	15-0
100	D0
102	D1
:	
112	D9
114	DA

Additionally, the readout order in each loop mode is as follows, assuming that sound data is read for each sample.

- Loop OFF

```
D0→D1→D2→・・・・→DA
```

- Loop ON

```
D0→D1→D2→・・・・→DA→D5→D6→・・・・→DA→D5→・・・
```

Notes on loop processing

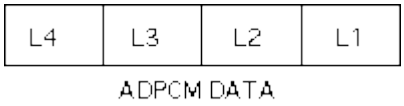
- Loop processing is premised on data corresponding to LSA and LEA (for ADPCM, data after decoding) having the same value. Hence, (for ADPCM, data after encoding), if necessary, make the settings so they have the same value (data prior to encoding).
- If the pitch is raised for short loop data (waveform data having few extremes that corresponds to the loop--data from LSA through LEA), it is possible that data corresponding to the loop section may not be read out at all. In this case, loop processing cannot be done correctly. To enable processing, the values will have to be set so that LEA-LSA >= OCT (with code) - 2, in view of the effect of pitch such as FNS and PLFO.

ADPCM

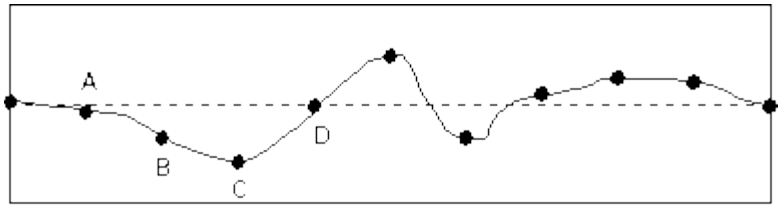
This LSI uses the Adaptive Differential Pulse Code Modulation (ADPCM) format for the sound data compression function. ADPCM is a data compression format that prevents sound quality from deteriorating by codifying, based on a quantized width adapted flexibly to changes in the waveform created from the difference between the sound data and the predicted data.

Method of Encoding

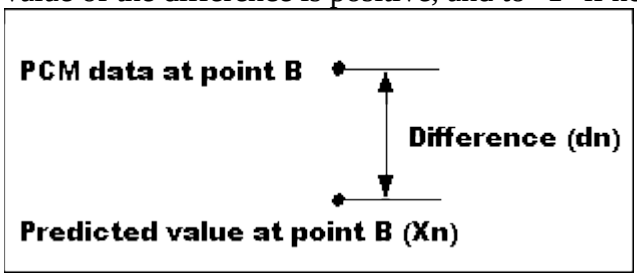
This LSI turns four-bit ADPCM data into 16-bit PCM data. Encoding is done by the procedure below.



1. Data to be encoded is converted to 16-bit PCM data each sampling cycle.



2. PCM data at point B and the predicted value (Xn) at point B are compared, and the difference (dn) found. At this time, the MSB (L4) of the ADPCM data is set to "0" if the value of the difference is positive, and to "1" if negative.



3. Next, the quantized width (Δn) and the absolute value of the difference (| dn |) are compared, and the remaining three ADPCM data bits (L3, L2, L1) for point B are decided from the ADPCM data correspondence table in Table 1.

- **Example 1**
  When the difference | dn | is the quantized width (Δn) * 7/4, as in Fig. a, the remaining three bits of ADPCM data become L3 = 1, L2 = 1, L1 = 1.

- **Example 2**
  When the difference | dn | is the quantized width (Δn) * 5/4, as in Fig. b, the remaining three bits of ADPCM data become L3 = 1, L2 = 0, L1 = 1.

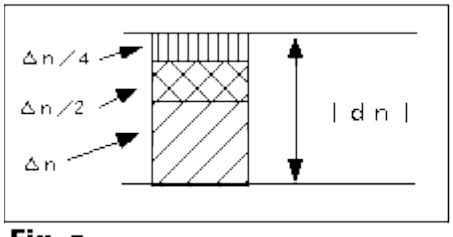


Fig. a

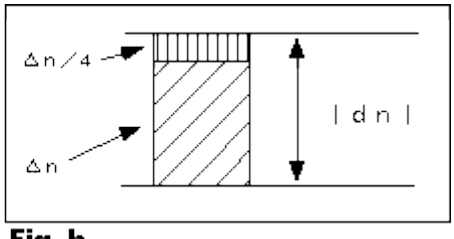


Fig. b

4. When the ADPCM data for point B is obtained, the ADPCM data for point C is found by getting the predicted value for point C (Xn + 1) and the quantized width for point C (Δ = 1).

    - The predicted value for point C (Xn + 1) = (1 - 2 * L4) * (L3 + L2/2 +L1/4 + 1/8) * quantized width (Δn) + predicted value (Xn) for point B.

    - The quantized width (Δn + 1) = f (L3, L2, L1) * quantized width (Δn)
      - f (L3, L2, L1) is the rate of change in the quantized width found from Table 2. Further, the initial value of the predicted value is zero; the initial value of the quantized width is 127, its minimum value is 127, and its maximum value is 24576.

ADPCM encoding data is obtained by repeating the above procedure.

Table 1:ADPCM data correspondence table

L4		L3	L2	L1	条件
dn≧0	dn≦0				
0	1	0	0	0	｜ｄｎ｜＜△ｎ／４
		0	0	1	△ｎ／４≦｜ｄｎ｜＜△ｎ／２
		0	1	0	△ｎ／２≦｜ｄｎ｜＜△ｎ＊３／４
		0	1	1	△ｎ＊３／４≦｜ｄｎ｜＜△ｎ
		1	0	0	△ｎ≦｜ｄｎ｜＜△ｎ＊５／４
		1	0	1	△ｎ＊５／４≦｜ｄｎ｜＜△ｎ＊３／２
		1	1	0	△ｎ＊３／２≦｜ｄｎ｜＜△ｎ＊７／４
		1	1	1	△ｎ＊７／４≦｜ｄｎ｜

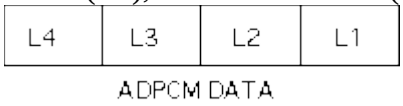
Table 2:Rate of transition in quantized width

L3	L2	L1	f
0	0	0	0.8984375
0	0	1	0.8984375
0	1	0	0.8984375
0	1	1	0.8984375
1	0	0	1.19921875
1	0	1	1.59765625
1	1	0	2.0
1	1	1	2.3984375

Method of Decoding

The decoding method is found in the same way as the predicted value and quantized width are found for encoding. The procedure is as below.

1. The decode value (Xn) at point B is found from the four-bit ADPCM data, quantized width (Δn), and decode value (Xn - 1) at point A.



The decode value (Xn) at point B = (1 - 2 * L4) * (L3 + L2/2 +L1/4 + 1/8) * quantized width (Δn) + decode value (Xn - 1) at point A.

2. Next, to find the decode value (Xn + 1) at point C, the quantized width (Δn + 1) is updated.

   The quantized width (Δn + 1) = f(L3, L2, L1) * quantized width (Δn).

Decoding is done by repeating the above procedure.

AEG

AEG transition rate change by the key scalling value. Execution rate is found from the following equation,and the real transition time is found from the transition time corresponding to the excution rate value on the time.
Execution rate and AEG transition time

Execution rate = (KRS[3:0]+OCT[3:0] * 2 + FNS[9] + rate [register setting value]) * 2
There are each register value within the bounds of following.

```
KRS[3:0]:+0 ~ +F[H]
OCT[3:0]:-8 ~ +7[H]
FNS[9]  :+0 , +1[H]
rate[register setting value]):+0 ~ +1F[H]
```

Attack Status			
Effective rate	**Transition time[ms] [-96dB~0dB]**	**Effective rate**	**Transition time[ms] [-96dB~0dB]**
0	infinity	**32**	47.0
1	infinity	**33**	38.0
2	8100.0	**34**	31.0
3	6900.0	**35**	27.0
4	6000.0	**36**	24.0
5	4800.0	**37**	19.0
6	4000.0	**38**	15.0
7	3400.0	**39**	13.0
8	3000.0	**40**	12.0
9	2400.0	**41**	9.4
10	2000.0	**42**	7.9
11	1700.0	**43**	6.8
12	1500.0	**44**	6.0
13	1200.0	**45**	4.7
14	1000.0	**46**	3.8
15	860.0	**47**	3.4
16	760.0	**48**	3.0
17	600.0	**49**	2.4
18	500.0	**50**	2.0

19	430.0	**51**	1.8
20	380.0	**52**	1.6
21	300.0	**53**	1.3
22	250.0	**54**	1.1
23	220.0	**55**	0.93
24	190.0	**56**	0.85
25	150.0	**57**	0.65
26	130.0	**58**	0.53
27	110.0	**59**	0.44
28	95.0	**60**	0.40
29	76.0	**61**	0.35
30	63.0	**62**	0.0
31	55.0	**63**	0.0

Decay 1, Decay 2, Release Status			
Effective rate	**Transition time[ms] [0dB~-96dB]**	**Effective rate**	**Transition time[ms] [0dB~-96dB]**
0	infinity	**32**	690.0
1	infinity	**33**	550.0
2	118200.0	**34**	460.0
3	101300.0	**35**	390.0
4	88600.0	**36**	340.0
5	70900.0	**37**	270.0
6	59100.0	**38**	230.0
7	50700.0	**39**	200.0
8	44300.0	**40**	170.0
9	35500.0	**41**	140.0
10	29600.0	**42**	110.0
11	25300.0	**43**	98.0
12	22200.0	**44**	85.0
13	17700.0	**45**	68.0
14	14800.0	**46**	57.0
15	12700.0	**47**	49.0
16	11100.0	**48**	43.0
17	8900.0	**49**	34.0
18	7400.0	**50**	28.0
19	6300.0	**51**	25.0
20	5500.0	**52**	22.0
21	4400.0	**53**	18.0
22	3700.0	**54**	14.0
23	3200.0	**55**	12.0
24	2800.0	**56**	11.0
25	2200.0	**57**	8.5

26	1800.0	**58**	7.1
27	1600.0	**59**	6.1
28	1400.0	**60**	5.4
29	1100.0	**61**	4.3
30	920.0	**62**	3.6
31	790.0	**63**	3.1

PG

- **Settings for OCT [3:0]**
  Specifies octave as two's complement. Values in parentheses are +1 octave for ADPCM.

OCT	**8**	**9**	**A**	**B**	**C**	**D**	**E**	**F**	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
Tone	-8	-7	-6	-5	-4	-3	-2	-1	0	+1	(+2)	(+3)	(+4)	(+5)	(+6)	(+7)

- Settings for FNS and OCT (The example gives settings for the F number table when the C4 note has been sampled at 44.1 KHz.)
  Putting the above in a different form, FNS[DEC] = 210 * (2P / 1200 - 1)

Note	**Note No.**	**Pitch P[CENT]**	**FNS[9:0] [DEC]**	**FNS[9:0] [X]**	**OCT[3:0] [X]**
B3	59	-100	909.1	38D	F
C4	60	0	0.0	0	0
C4#	61	100	60.9	3D	0
D4	62	200	125.4	7D	0
D4#	63	300	193.7	C2	0
E4	64	400	266.2	10A	0
F4	65	500	342.9	157	0
F4#	66	600	424.2	1A8	0
G4	67	700	510.3	1FE	0
G4#	68	800	601.5	25A	0
A4	69	900	698.2	2BA	0
A4#	70	1000	800.6	321	0
B4	71	1100	909.1	38D	0
C5	72	0	0.0	0	1

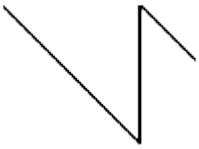
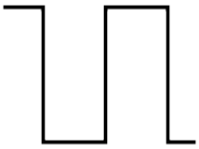
LFO

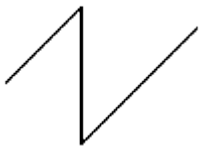
- **Frequencies generated by LFOF [4:0]**

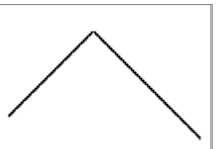
LFO[4:0]	**frequencie [Hz]**	**LFO[4:0]**	**frequencie [Hz]**
00	0.17	**10**	2.87
01	0.19	**11**	3.31
02	0.23	**12**	3.92
03	0.27	**13**	4.79
04	0.34	**14**	6.15
05	0.39	**15**	7.18
06	0.45	**16**	8.60

07	0.55	**17**	10.80
08	0.68	**18**	14.40
09	0.78	**19**	17.20
0A	0.92	**1A**	21.50
0B	1.10	**1B**	28.70
0C	1.39	**1C**	43.10
0D	1.60	**1D**	57.40
0E	1.87	**1E**	86.10
0F	2.27	**1F**	172.30

- **Form of ALFO wave by ALFOWS [1:0]**
- **Form of PLFO wave by PLFOWS [1:0]**

ALFOWS [X]	**AM modulation (ALFO)**		
	Volume	**ALFO[7:0]**	**ALFO wave**
0	-0dB : : : : :	00 : : : : FF	
1	-0dB : : : : :	00 : : : : FF	
2	-0dB : : : : :	00 : : : : FF	
3	-0dB : : : : :	00 : : : : FF	

PLFOWS [X]	**PM modulation (PLFO)**		
	Pitch	**PLFO[7:0]**	**PLFO wave**
0	+ : 0 : -	7F : 00 : 80	
1	+ : 0 : -	7F : 00 : 80	

2	+ : 0 : -	7F : 00 : 80	
3	+ : 0 : -	7F : 00 : 80	

- **Extent of mixing by ALFOS [2:0]**
- **Extent of effect on pitch by PLFOS [2:0]**

ALFO[X]	Mixing for EG
0	No effect
1	-.4dB displacement
2	-.8dB displacement
3	-1.5dB displacement
4	-3.0dB displacement
5	-6.0dB displacement
6	-12.0dB displacement
7	-24.0dB displacement

PLFO[X]	Effect on pitch
0	No effect
1	- 3 ~ + 2 CENT displacement
2	- 7 ~ + 5 CENT displacement
3	- 14 ~ + 12 CENT displacement
4	- 27 ~ + 25 CENT displacement
5	- 55 ~ + 52 CENT displacement
6	- 112 ~ + 103 CENT displacement
7	- 231 ~ + 202 CENT displacement

Mixer

- **Volume and registers**

TL[7:0]

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Volume	-48dB	-24dB	-12dB	-6dB	-3dB	-1.5dB	-0.8dB	-0.4dB

IMXL[3:0],DISDL[3:0],EFSDL[3:0],MVOL[3:0]

Register	Volume
0	-MAX dB
1	-42 dB
2	-39 dB
:	:
D	-6 dB

E	-3 dB
F	0 dB

DIPAN[4:0],EFPAN[4:0]

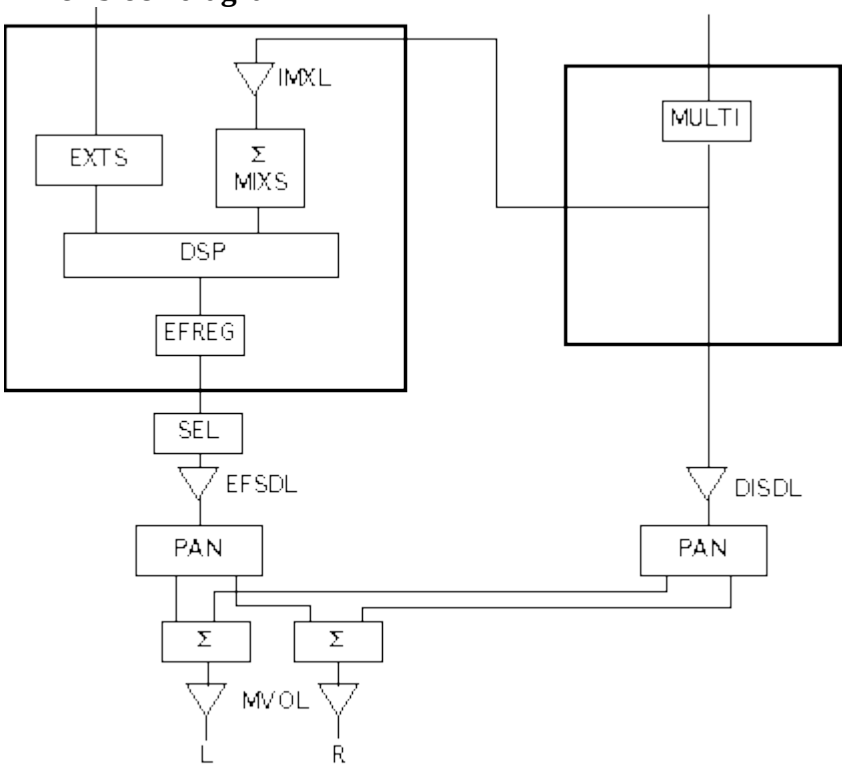
Register	L	R
0	0 dB	0 dB
1	-3 dB	0 dB
2	-6 dB	0 dB
:	:	:
D	-39 dB	0 dB
E	-42 dB	0 dB
F	-MAX dB	0 dB

Register	L	R
10	0 dB	0 dB
11	0 dB	-3 dB
12	0 dB	-6 dB
:	:	:
1D	0 dB	-39 dB
1E	0 dB	-42 dB
1F	0 dB	-MAX dB

- Correspondence between effect sources and slots that EFSDL and EFPAN should set

Slot	Output mixer source data
0..F	EFREG[0]..EFREG[15]
10	Digital audio 1L
11	Digital audio 1R

- **Mixer block diagram**



FEG

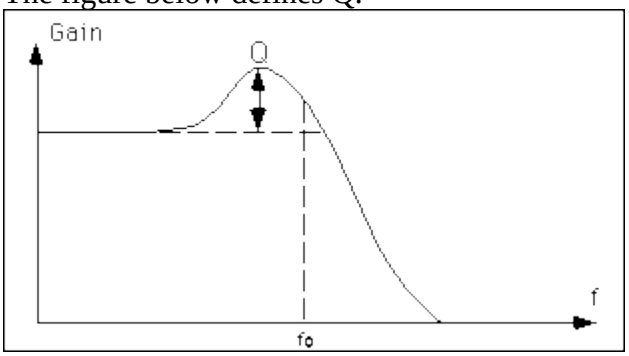
The IIR filter enables LPF to pass through each channel.
The dedicated EG enables time variance of the LPG cutoff frequency.
LPF supports fixed (no time variance) Q (resonance) setting for each channel.

Q [12:0]Resonance data

Sets Q for the FEG filter. Setting can be done from 0 through 48 dB. The relationships between bits and gain are as below.

DATA	GAIN[dB]
Q12	48.0
Q11	24.0
Q10	12.0
Q9	6.0
Q8	3.0
Q7	1.5
Q6	0.75
Q5	0.375
Q4	0.375/ 2
Q3	0.375/ 4
Q2	0.375/ 8
Q1	0.375/16
Q0	0.375/32

The figure below defines Q.



FAR [4:0]

Specifies the rate of the FEG transition in attack status.

FD1R [4:0]

Specifies the rate of the FEG transition in decay 1 status.

FD2R [4:0]

Specifies the rate of the FEG transition in decay 2 status.

FRR [4:0]

Specifies the rate of the FEG transition in release status.
The rate and transition time for each register is the same as for AEG.

FLV0 [12:0]

Cutoff frequency at attack start

FLV1 [12:0]

Cutoff frequency at attack end (when decay starts)

FLV2 [12:0]

Cutoff frequency at decay end (when sustain starts)

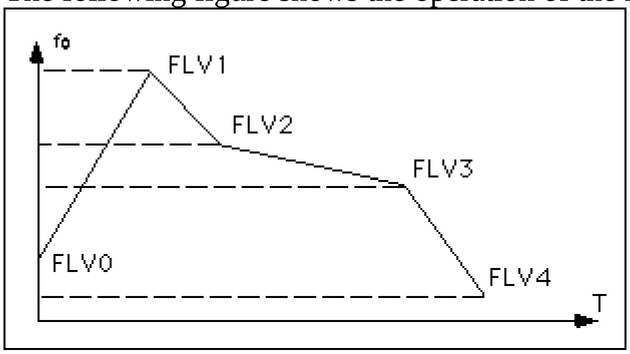
FLV3 [12:0]

Cutoff frequency at KOFF

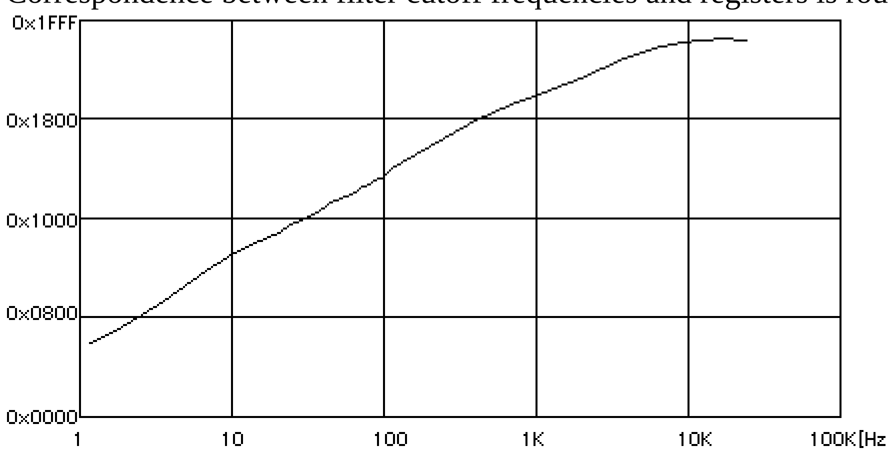
FLV4 [12:0]

Cutoff frequency after release

The following figure shows the operation of the registers.



Correspondence between filter cutoff frequencies and registers is roughly as below.



FAR [4:0]

Specifies the rate of transition of FEG in attack status. (Volume transition is increased.)

FD1R [4:0]

Specifies the rate of transition of FEG in decay 1 status. (Volume transition is decreased.)

FD2R [4:0]

Specifies the rate of transition of FEG in decay 2 status. (Volume transition is decreased.)

FRR [4:0]

Specifies the rate of transition of FEG in release status. (Volume transition is decreased.)

Execution rate and FEG transition time

- -

Effective rate = (KRS[3:0] + OCT[3:0]) * 2
+ FNS[9] + (rate [register setting value]) * 2

KRS[3:0] : 0 ... F
OCT[3:0] : -8 ... +7
FNS[9] : +0 , +1
rate [register setting value] : +00 ... +1F

Effective rate	Transition time [ms]	Effective rate	Transition time [ms]
0	infinity	**32**	690.0
1	infinity	**33**	550.0
2	118200.0	**34**	460.0
3	101300.0	**35**	390.0
4	88600.0	**36**	340.0
5	70900.0	**37**	270.0
6	59100.0	**38**	230.0
7	50700.0	**39**	200.0
8	44300.0	**40**	170.0
9	35500.0	**41**	140.0
10	29600.0	**42**	110.0
11	25300.0	**43**	98.0
12	22200.0	**44**	85.0
13	17700.0	**45**	68.0
14	14800.0	**46**	57.0
15	12700.0	**47**	49.0
16	11100.0	**48**	43.0
17	8900.0	**49**	34.0
18	7400.0	**50**	28.0
19	6300.0	**51**	25.0
20	5500.0	**52**	22.0
21	4400.0	**53**	18.0
22	3700.0	**54**	14.0
23	3200.0	**55**	12.0
24	2800.0	**56**	11.0
25	2200.0	**57**	8.5
26	1800.0	**58**	7.1
27	1600.0	**59**	6.1
28	1400.0	**60**	5.4
29	1100.0	**61**	4.3
30	920.0	**62**	3.6
31	790.0	**63**	3.1

DSP

RBL [1:0] (W):

Specifies length of ring buffer.

RBL[1:0]ring buffer	
0	8 Kwords
1	16 Kwords
2	32 Kwords
3	64 Kwords

RBP [22:11] (W):

Specifies leading address of ring buffer. (4 Kword limit)

Generates modulation waveform used with DSP

The wave signal for modulation used with DSP can be generated by the following three means:

1. The CPU writes the modulation wave to the DSP memory (COEF).
2. Wave data for modulation is held in the sound memory, is produced as sound lower than the usual pitch, and the data buffered in MIXS is used as the modulation wave.
3. The CPU writes the modulation wave to the DSP memory (MEMS).

- Method **1** has a precision of 13 bits, which puts a load on the CPU, but enables waveforms to be created freely.
- Method **2** has a precision of 16 bits, so that the amplitude and pitch can be changed by EG and LFO. (However, when the SDIR is set to "1", EG = 000 [X], ALFOS = 0 [X], and TL - 00 [X], which is equivalent to a precision of 20 bits.)
- Method **3** has a precision of 24 bits, which puts a load on the CPU, but enables waveforms to be created freely.

RAM in DSP

MIXS [19:0] (R/W):

Data buffer for sound from input mixer. (Data quantity:16)

Note:

Writing to MIXS [19:0] is used for LSI tests. Writing other than in test mode is invalid for the following reasons:

- Regardless of the setting, data is constantly being written from the sound source.
- A second generation's worth of data is held for adding all slots, but the generation cannot be specified at access.

EXTS [15:0] (R):

Data buffer for digital audio input. (Data quantity:2)

MEMS [23:0] (R/W):

Data buffer for digital audio input. (Data quantity:32)
(Data is actually written to MEMS [7:0] at the same time as data is written to MEMS[23:16].)

With the DSP program, only one of the above three buffers can be selected as input data INPUTS.
Further, the difference in bit length is adjusted by shifting to the high order.

All three buffers above can be accessed from the CPU; the access timing is as below. (Timing (T0&T1, T2&T3,...) is equivalent to one step of DSP.)

	T0	T1	T2	T3	T4	T5	T6	T7
MIXS	DSPR	**IMXRD**	DSPR	DMSP	DSPR	**IMXWT**	DSPR	DMSP
EXTS	DSPR	DMSP	DSPR	DMSP	DSPR	DMSP	DSPR	DMSP
MEMS	DSPR	DMSP	DSPR	DMSP/DSPW	DSPR	DMSP	DSPR	DMSP/DSP

```
DMSP  : READ/WRITE BY DMA,MCPU,SCPU
DSPR  : READ BY DSP
DSPW  : WRITE BY DSP
IMXRD : READ MIXS.
IMXWT : WRITE TO MIXS.
```

Caution:
Standby for a request to access MIXS via DMSP can be implemented with T1 and T5. T2&T3 and T6&T7 are the sound memory read timing for PCM sound data, so DSP cannot be accessed. Hence, the request to access sound memory via DSP must be coded in odd steps (lines 2, 4, 6,...).

TEMP [23:0] (R/W):
DSP work buffer. (Data quantity: 128)
Configured as a ring buffer. The pointer decrements by 1 for each sample.

COEF [12:0] (R/W):
Buffer for coefficient data quantity. (Data quantity: 128)

Caution:
To maintain compatibility in the future when the data width is expanded to 16 bits, write "0" to the three low-order bits not defined in the register map.

MADRS [16:1] (R/W):
DSP address buffer. (Data quantity: 64)

MPRO [63:0] (R/W):
DSP microprogram buffer. (Data quantity: 128)

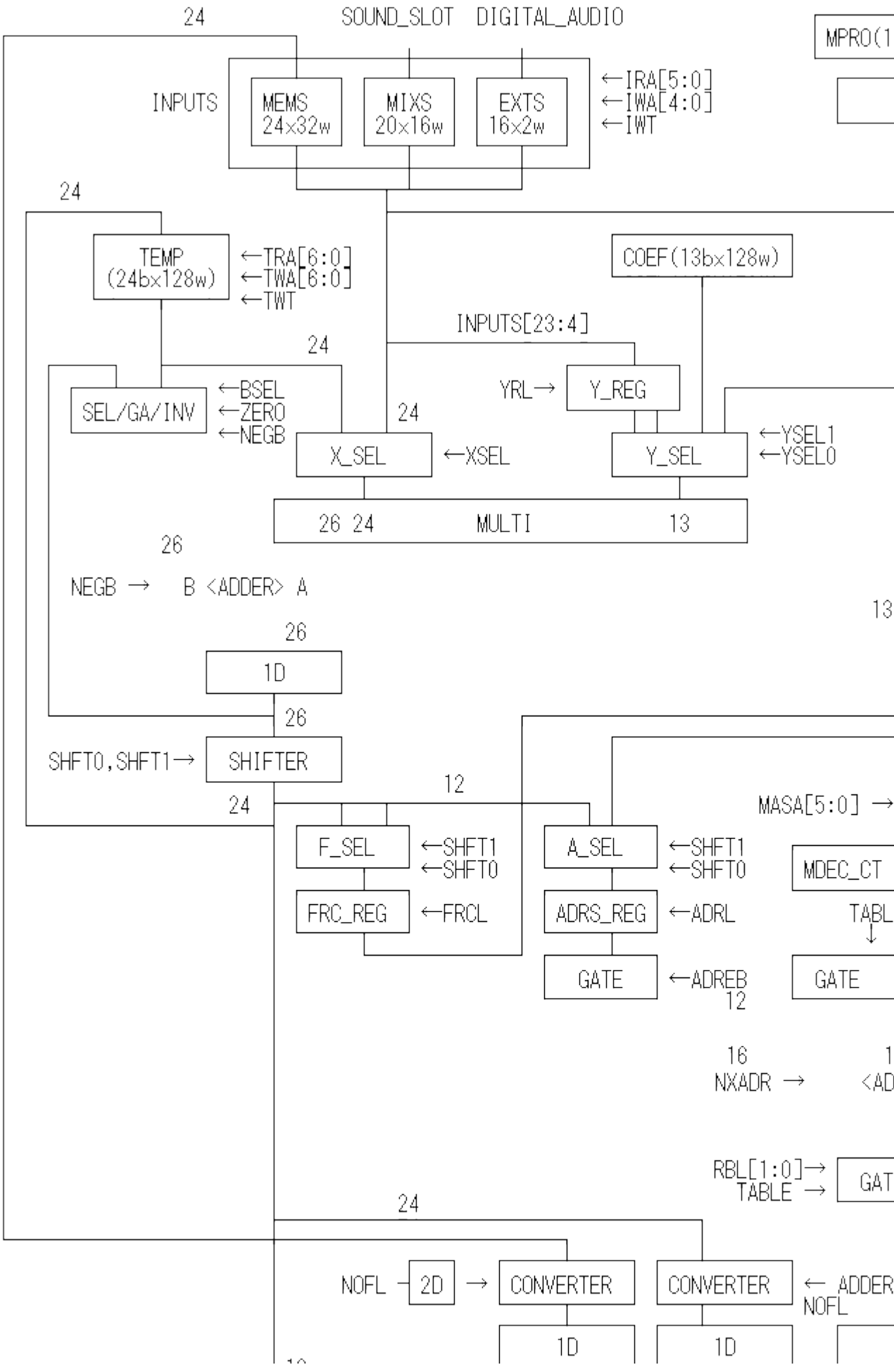
EFREG [15:0] R/W:
DSP output buffer. (Data quantity: 16)

All five buffers above can be accessed from the CPU, and the access timing is as below. (Timing (T0&T1, T2&T3,...) is equivalent to one step of DSP.)

	T0	T1	T2	T3	T4	T5	T6	T
TEMP	DSPR	DMSP/DSPW	DSPR	DMSP/DSPW	DSPR	DMSP/DSPW	DSPR	DMSP/
COEF	DSPR	DMSP	DSPR	DMSP	DSPR	DMSP	DSPR	DMSP
MADRS	DSPR	DMSP	DSPR	DMSP	DSPR	DMSP	DSPR	DMSP
MPRO	DSPR	DMSP	DSPR	DMSP	DSPR	DMSP	DSPR	DMSP
EFREG	MIXR	DMSP/DSPW	----	DMSP/DSPW	----	DMSP/DSPW	----	DMSP/

```
MIXR: READ BY OUTPUT MIXTER.
```

Configuration of DSP


24
SOUND_SLOT DIGITAL_AUDIO
MPRO(1
INPUTS
MEMS 24×32w
MIXS 20×16w
EXTS 16×2w
←IRA[5:0]
←IWA[4:0]
←IWT
24
TEMP (24b×128w)
←TRA[6:0]
←TWA[6:0]
←TWT
COEF(13b×128w)
INPUTS[23:4]
24
SEL/GA/INV
←BSEL
←ZERO
←NEGB
YRL→
Y_REG
24
X_SEL
←XSEL
Y_SEL
←YSEL1
←YSEL0
26 24
MULTI
13
26
NEGB →
B <ADDER> A
13
26
1D
26
SHFT0,SHFT1→
SHIFTER
12
24
MASA[5:0] →
F_SEL
←SHFT1
←SHFT0
A_SEL
←SHFT1
←SHFT0
MDEC_CT
FRC_REG
←FRCL
ADRS_REG
←ADRL
TABL
GATE
←ADREB
12
GATE
16
NXADR →
1
<AD
RBL[1:0]→
TABLE →
GAT
24
NOFL
2D
→
CONVERTER
CONVERTER
← ADDER
NOFL
1D
1D

Overview of DSP Program (total of 55 bits)

MASA [5:0]:
Specifies the MADRS read address.

IWA [4:0]:
Specifies the write address for input data (INPUTS).

IWT:
Requests an interrupt for DSP input data.

IRA [5:0]:
Specifies the read address for input data (INPUTS) .
INPUTS map (Address is DSP program address)

Address	Contents of INPUTS
00[X]..1F[X]	MEMS
20[X]..2F[X]	MIXS
30[X]	EXTS0(L)
31[X]	EXTS0(R)
32[X]..37[X]	For expansion (cannot be specified)
38[X]..3F[X]	Undefined (cannot be specified)

TWA [6:0]:
Specifies the TEMP write address.

TWT:
Requests write of TEMP input data.

TRA [6:0]:
Specifies the TEMP read address.

EWA [3:0]:
Specifies the EFREG address for output.

EWT:
Requests write of output data to EFREG.

BSEL:
0 = Select TEMP data; 1 = Select accumulator.

ZERO:
1 = Set adder input to "0".

NEGB:
0 = Add; 1 = Subtract.

YRL:
Latches INPUTS [23:4]. (Latch data can be used from the next step.)

YSEL1: Select 1 for multiplier's Y input.
YSEL0: Select 0 for multiplier's Y input.

YSEL1	YSEL0	Input selected

0	0	FRC_REG
0	1	COEF
1	0	Y_REG[23:11]
1	1	"0" | Y_REG[15:4] **(MSB=0)**

XSEL:

Selects multiplier's X input.

- 0 = Select TEMP data
- 1 = Select INPUTS data.

MRD:

Sound memory read request. (Request is permitted for odd steps only.)

MWT:

Sound memory write request. (Request is permitted for odd steps only.)

Caution:

Flags associated with memory access (MRD, MWT, NOFL, TABLE, NXADR, ADREB, and MASA [4:0]) are permitted only in odd steps (lines 2, 4, 6...) of microprograms.

NOFL:

1 = Floating conversion not done when sound memory is accessed. This flag is set to "1" for storing linear format data in sound memory.

TABLE:

1 = Subtract counter (MDEC_CT) is the output gate, and the output is "0".
This is for when the reason for use is something other than as a ring buffer for sound memory (e.g., when using as a filter coefficient table).
Further, in this case, there is no restriction on the size of the ring buffer by RBL.
MDEC_CT is decremented by one each sampling, and when it reaches 0 the value corresponding to the loop length specified by RBL is loaded.

NXADR:

Adds 1 to the memory address.
For temporary interpolation mode, NXADR is used, the adjacent values are used, and interpolation done.

ADREB:

0 = Address register (ADRS_REG) is the output gate, and the output is "0". This is used for writing data to the ring buffer.

SHFT1: Shifter control 1
SHFT0: Shifter control 0

SHFT1	SHFT0	Shift amount	For overflow
0	0	X1	Protected
0	1	X2	Protected
1	0	X2	Not protected
1	1	X1	Not protected

FRCL:

Memory address decimal latch (used in interpolation mode)

ADRL:

Memory address integer latch

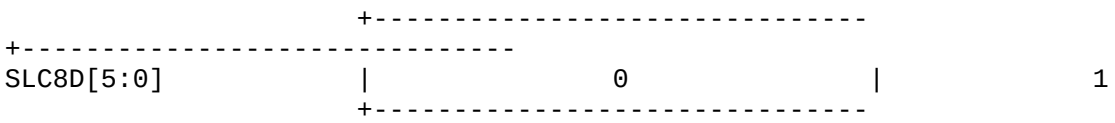
Data that can be selected by F_SEL and A_SEL in interpolation mode (SHFT1 = SHFT0 = 1) and non-interpolation mode (SHFT {symbol} SHFT0 {symbol} 1) is as follows:

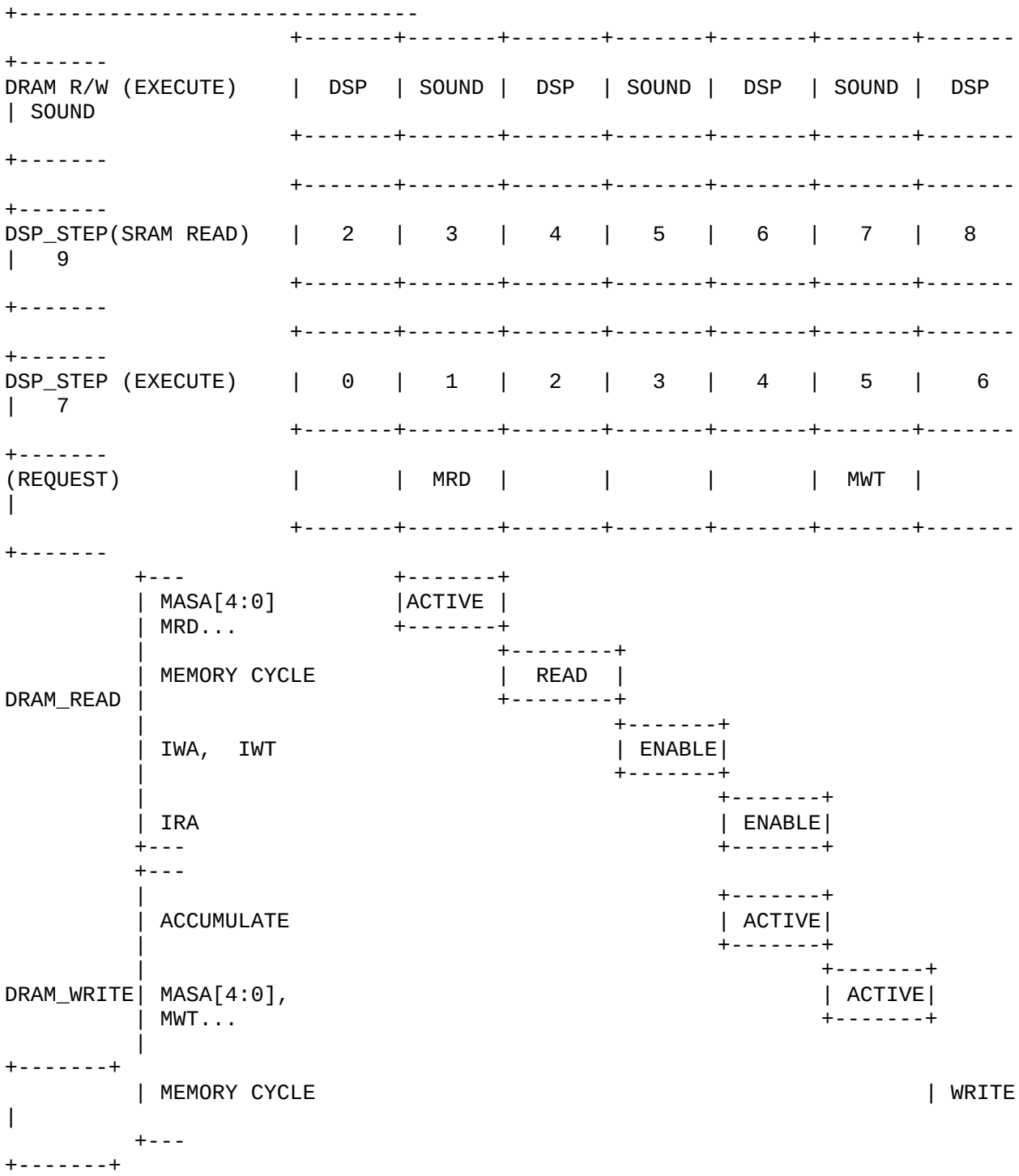
F_SEL		
Register output	**Non-interpolation mode**	**Interpolation mode**
FRC_REG12	SFTREG23	"0"
FRC_REG11	SFTREG22	SFTREG11
FRC_REG10	SFTREG21	SFTREG10
FRC_REG9	SFTREG20	SFTREG9
FRC_REG8	SFTREG19	SFTREG8
FRC_REG7	SFTREG18	SFTREG7
FRC_REG6	SFTREG17	SFTREG6
FRC_REG5	SFTREG16	SFTREG5
FRC_REG4	SFTREG15	SFTREG4
FRC_REG3	SFTREG14	SFTREG3
FRC_REG2	SFTREG13	SFTREG2
FRC_REG1	SFTREG12	SFTREG1
FRC_REG0	SFTREG11	SFTREG0
A_SEL		
Register output	**Non-interpolation mode**	**Interpolation mode**
ADRS_REG11	INPUTS23	SFTREG23
ADRS_REG10	INPUTS23	SFTREG22
ADRS_REG9	INPUTS23	SFTREG21
ADRS_REG8	INPUTS23	SFTREG20
ADRS_REG7	INPUTS23	SFTREG19
ADRS_REG6	INPUTS22	SFTREG18
ADRS_REG5	INPUTS21	SFTREG17
ADRS_REG4	INPUTS20	SFTREG16
ADRS_REG3	INPUTS19	SFTREG15
ADRS_REG2	INPUTS18	SFTREG14
ADRS_REG1	INPUTS17	SFTREG13
ADRS_REG0	INPUTS16	SFTREG12

Interpolation mode is used when high-precision processing is required, such as for changing pitch.

Example:

DRAM access timing (in which the request is for read at step 1 and write at step 5.)

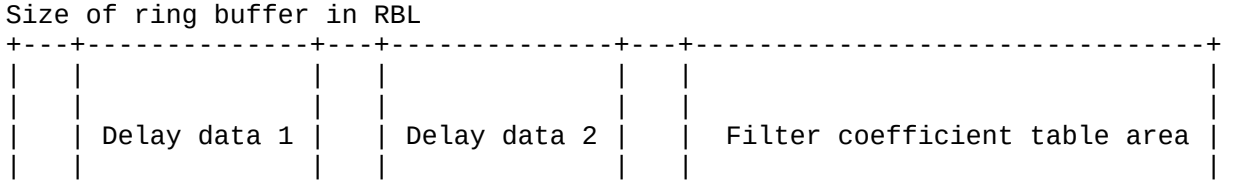


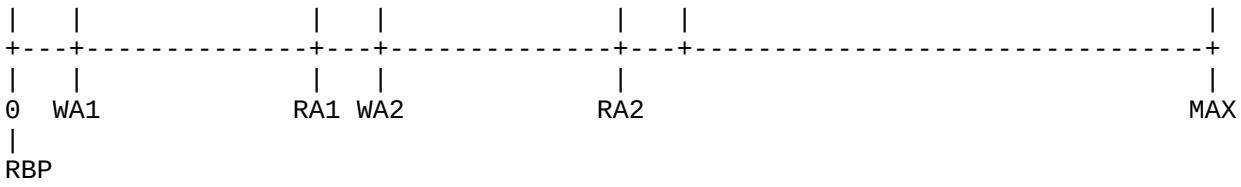


Note:
When read and write are specified simultaneously in the same step for INPUTS, TEMP, etc., write is executed after read.

Example of how to implement a ring buffer and filter table in DSP

DSP access space (64 K words maximum)





- WA1 is the delay data 1 write address; it can be written with ADREB = 0.
- RA1 is the delay data 1 read address. With ADREB= 0, a fixed time delay is obtained. With ADREB = 1, data can be obtained for the transition in delay time equivalent to the transition of ADRS_REG.
- WA2 and RA2 are associated with delay data 2, and must be separate from delay data 1. In particular, when memory is being read for ADREB = 1, both must be separated on account of the displacement in the addresses.
- The ring buffer area is accessed in the status TABLE = 0. Here, if the ring buffer size exceeds the relative access address (MADRS [16:1] + ADRS_REG [16:1] (+1)), this is wrapped around to 0. (However, to take account of modifications to the size of the ring buffer, it is recommended that wraparound be avoided.)

  Note:
  In this case, the actual access address is expressed as (MADRS[16:1] + ADRS_REG[16:1] + MDEC_CT[16:1] (+1)).
- The filter coefficient table area is accessed in the status TABLE = 1. Here, even if the ring buffer size exceeds the relative access address (MADRS [16:1] + ADRS_REG [16:1] (+1)), this is not wrapped around to 0. (However, the size is 64 K words maximum.)

Contents

Electrical Specifications

Absolute Maximum Ratings

Item	Code	Rating	Unit
Supply voltage	VDD	-0.5 ~ +7.0	V
Input voltage	VI	-0.5 ~ VDD+0.5	V
Output current	IO	-20 ~ +20	mA
Storage temperature	Tstg	-50 ~ +125	celsius

Recommended Operating Conditions

Code	Item	Minimum	Standard	Maximum	Unit
VDD	Supply voltage	4.75	5.00	5.25	V
VSS	Supply voltage	---	0	---	
VIL0	Low-level input voltage (TTL level input terminal)	-0.3	---	0.8	
VIH0	High-level input voltage (TTL level input terminal)	2.2	---	VDD+0.3	

VIL1	Low-level input voltage (CMOS level input terminal)	-0.3	---	0.3*VDD	
VIH1	High-level input voltage (CMOS level input terminal)	0.7*VDD	---	VDD+0.3	
Ta	Ambient operating temperature	0	---	70	celsius

Electrical Characteristics under Recommended Operating Conditions

Terminal capacity

Code	Item	Minimum	Standard	Maximum	Unit
VDD	Input terminal capacity	---	---	8	pF
VDD	Output terminal capacity	---	---	10	
VDD	I/O terminal capacity	---	---	12	

DC characteristics

Code	Item	Measurement conditions	Minimum	Standard	Maximum	Unit
VOL	Low-level output voltage	IOL= 1.0mA	---	---	0.4	V
VOH	High-level output voltage	IOH=-0.1mA	2.4	---	---	V
ILI	Input leak current		---	---	10	uA
ILO	Output leak current		---	---	25	uA
IDD	Consumption current		---	---	80	mA

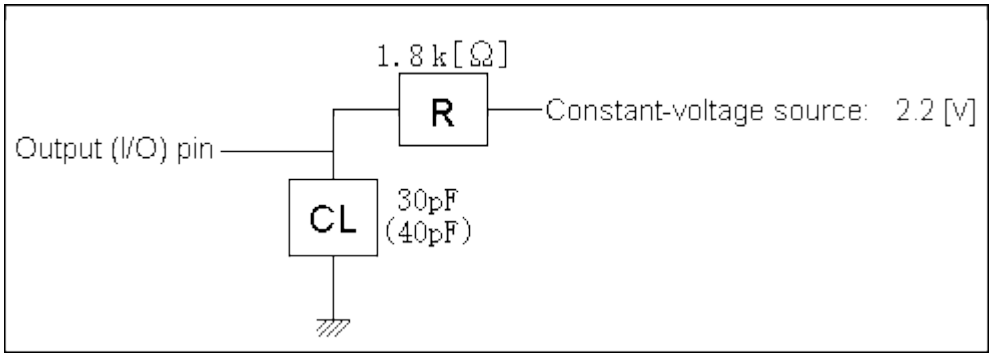
AC characteristics

(Measurement conditions)

1. Values of AC characteristics are results of measurements where the transition time of all input signals is 1 ns.
   (See the timing diagram "Signal transition time" below for the definition of the input transition time.)

2. The timing measurement level is 0.5* VDD [V], for the CMOS level interface, and 1.5 [V] for the TTL level interface.

3. Output load conditions. (The load circuit when AC characteristics were measured was as below.)



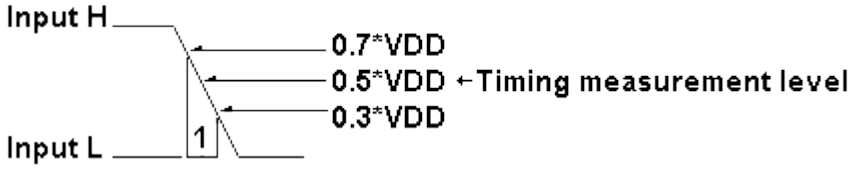
Note:

The capacity CL is the sum of the applied capacity, MCD [7:0] only--40 [pF].

Signal transition time

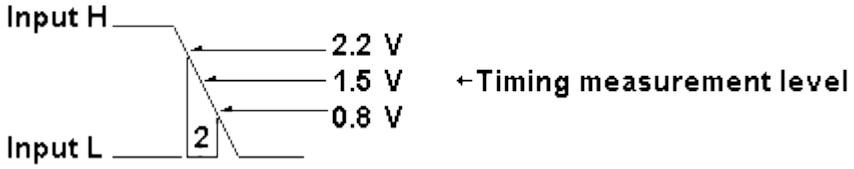
No.	Item	Measurement conditions	Minimum	Standard	Maximum	Unit
1	Transition time for CMOS level input (MACK, MCCK)	---	1	---	4	ns
2	Transition time for TTL level input (except MACK and MCCK)	---	1	---	4	
3	Transition time for output (MCD [7:0])	CL=40pF	1	---	4	
3	Transition time for output (except MCD [7:0])	CL=30pF	1	---	4	

1. CMOS level input conditions (MACK, MCCK)



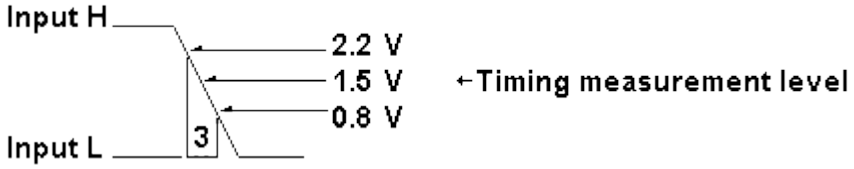
1: Transition time

2. TTL level input conditions (except MACK and MCCK)



2: Transition time

3. Output level conditions (all outputs are TTL level) and timing

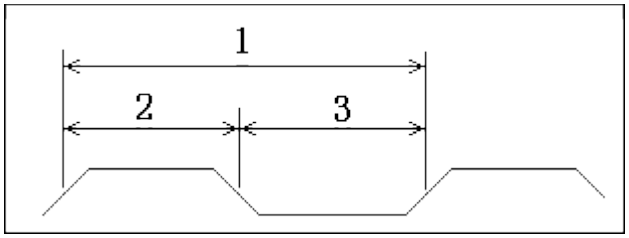


3: Transition time

MCCK timing

No.	Code	Item	Minimum	Standard	Maximum	Unit
-		MCCK input clock frequency	17	-	28.634	KHz
1	tCC	MCCK input clock cycle	35	-	59	ns
2		MCCK input clock high time	15	-	---	
3		MCCK input clock low time	15	-	---	

MCCK:

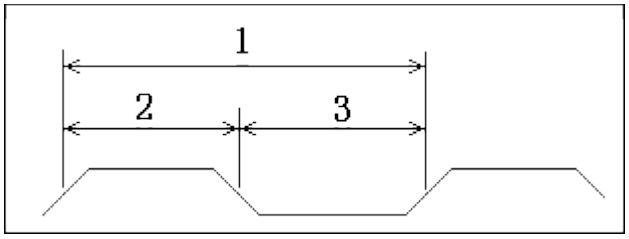


MACK timing

No.	Code	Item	Minimum	Standard	Maximum	Unit

-	fC	MACK input clock frequency	-	22.5792	-	KHz
1	tC	MACK input clock cycle	-	44.2885	-	ns
2	tCH	MACK input clock high time	19.5	-	24.5	
3	tCL	MACK input clock low time	19.5	-	24.5	

MACK:

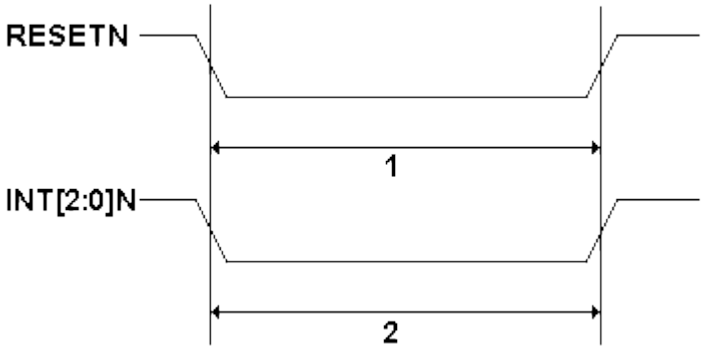


Reset, external interrupt request timing

No.	Code	Item	Measurement conditions	Minimum	Standard	Maximum	Unit
1	tPWR	Reset RESETN pulse time		tC+30	-	-	ns
2	tPWI	External interrupt "INT [2:0] N" request pulse width		2tC+30	-	-	

Caution

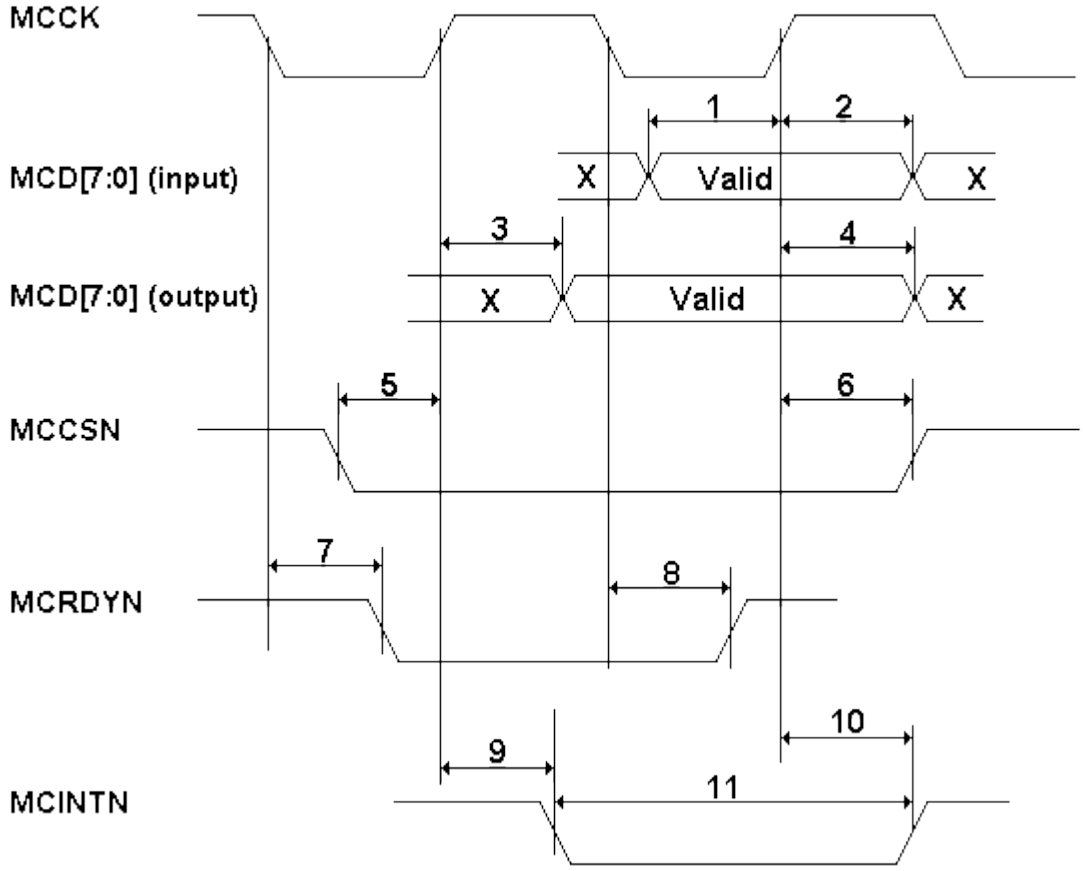
1. Input the reset pulse after the power supply stabilizes.
2. After the reset pulse rises, the initializing routine is executed inside the device for approximately 30 ms. During this period, access from the CPU is prohibited.



Main CPU interface timing

No.	Code	Item	Measurement conditions	Minimum	Standard	Maximum	Unit
1		MCD [7:0] input setup time	CL=40pF	9{6}	-	-	ns
2		MCD [7:0] input hold time		3{0}	-	-	
3		MCD [7:0] output delay time		-	-	25{21}	
4		MCD [7:0] output hold time		4{6}	-	-	
5		MCCSN input setup time	CL=30pF	9{6}	-	-	
6		MCCSN input hold time		3{0}	-	-	
7		MCRDYN output delay time		-	-	25{21}	
8		MCRDYN output hold time		4{6}	-	-	
9		MCINTN output delay time		-	-	25{21}	
10		MCINTN output hold time		4{7}	-	-	

11		MCINTN output pulse width		tCC-10	-	tCC+20	



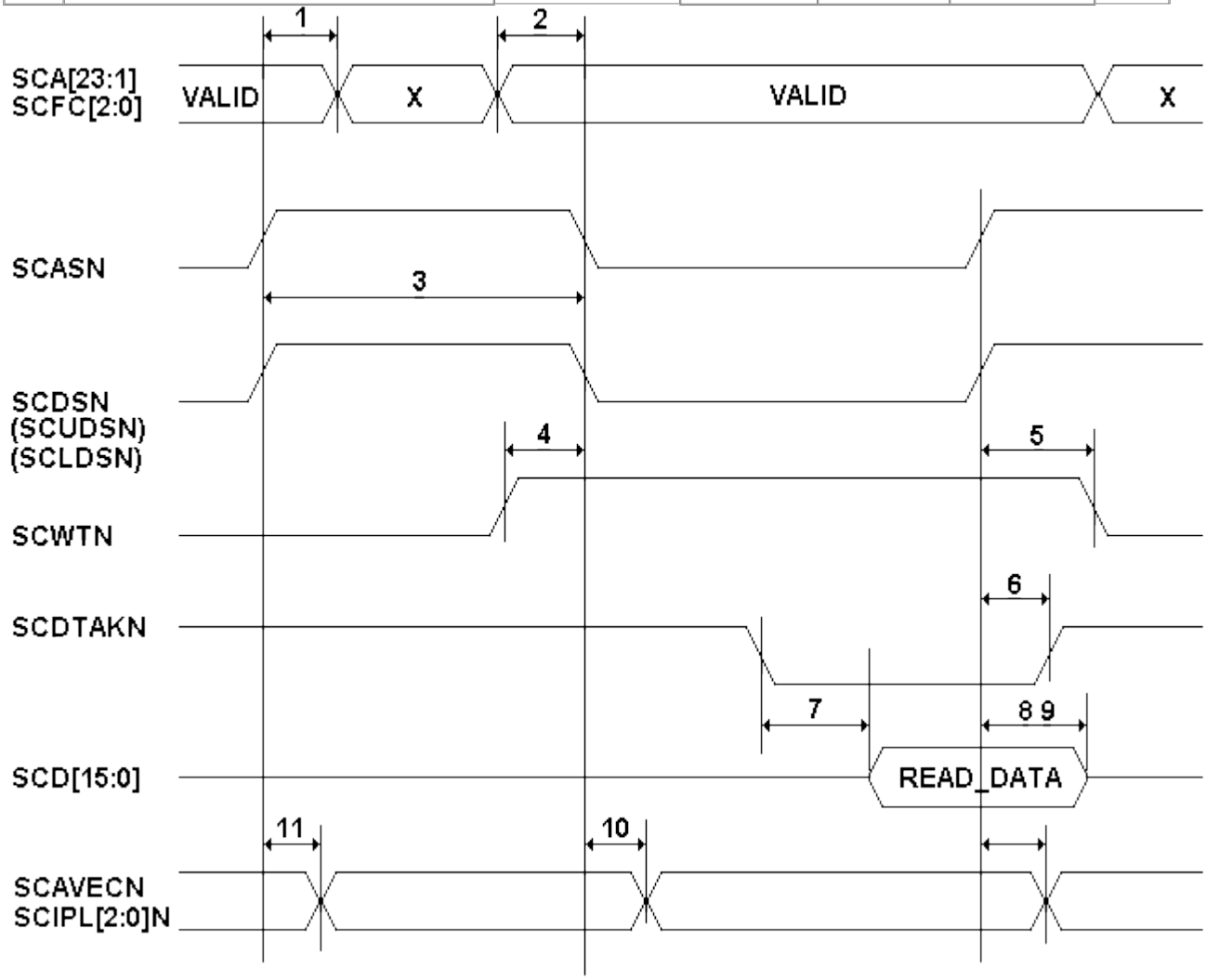
Caution:
The above timing chart shows the timing relationships for MCCK. It does not show the timing relationships among other signals.

Sound CPU interface timing

Sound CPU read

No.	Item	Measurement conditions	Minimum	Standard	Maximum	Unit
1	SCASN,SCDSN negated to SCA[23:1],SCFC[2:0] invalid.	CL=30pF	10{2}	-	-	ns
2	SCA[23:1],SCFC[2:0] valid to SCASN,SCDSN asserted.		10{-30}	-	-	
3	SCASN,SCDSN width negated.		60{}	-	-	
4	SCWTN high to SCASN,SCDSN asserted.		10{-33}	-	-	
5	SCASN,SCDSN negated to SCWTN low.		10{}	-	-	
6	SCASN,SCDSN negated to DTACKN negated.		0{3}	-	20{10}	
7	SCDTAKN asserted to READ_DATA vaild.		-	-	50{28}	
8	SCASN,SCDSN negated to		0{}	-	-	

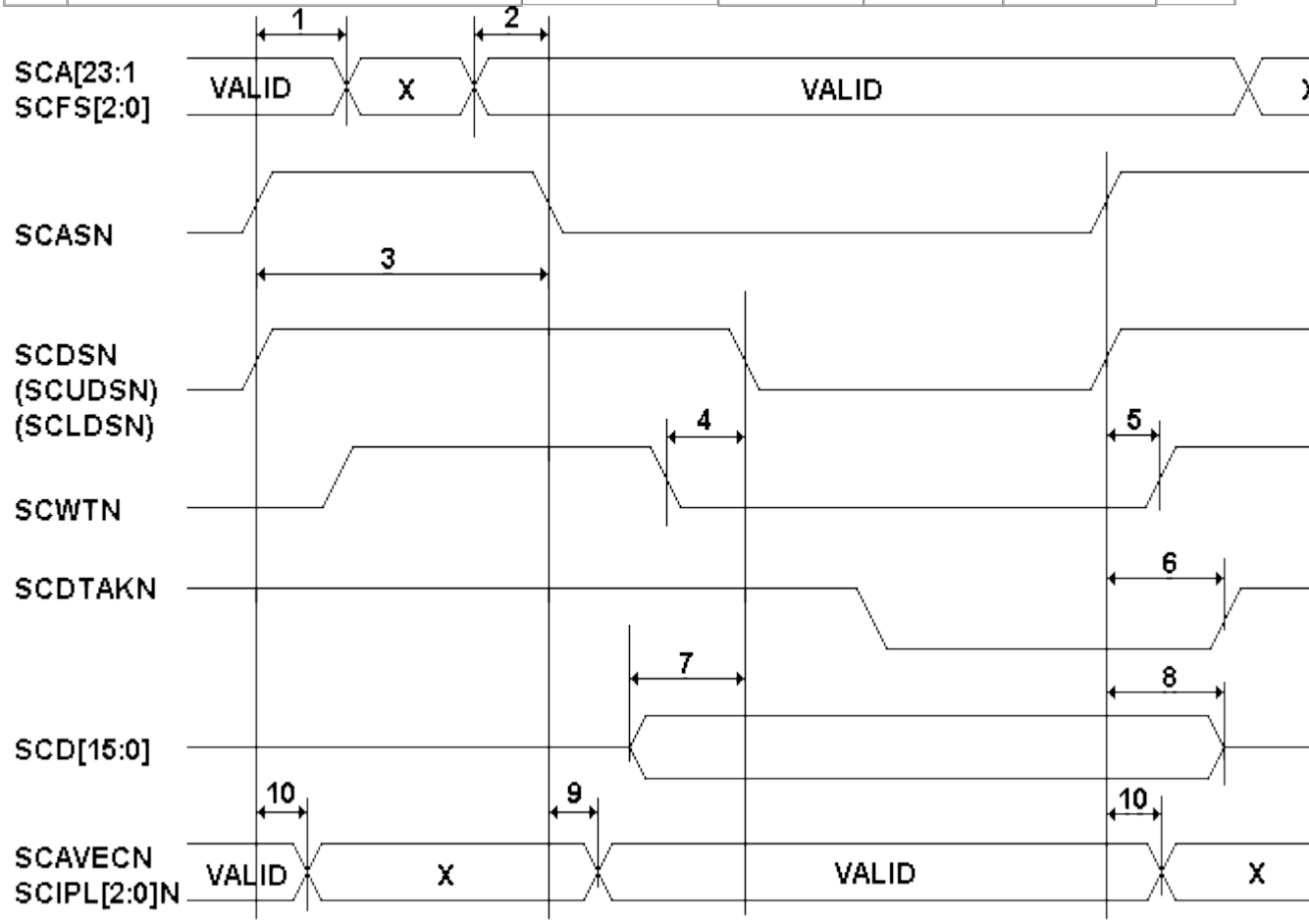
	READ_DATA negated.					
9	SCASN,SCDSN negated to data_out HI-Z.		-	-	60{}	
10	SCASN,SCDSN asserted to SCAVECN,SCIPL[2:0]N valid.		-	-	tC+40{64}	
11	SCASN,SCDSN negated to SCAVECN,SCIPL[2:0]N invalid.		0{8}	-	-	



Sound CPU write

No.	Item	Measurement conditions	Minimum	Standard	Maximum	Unit
1	SCASN,SCDSN negated to SCA[23:1],SCFC[2:0] invalid.	CL=30pF	10{2}	-	-	ns
2	SCA[23:1],SCFC[2:0] valid to SCASN,SCDSN asserted.		10{-30}	-	-	
3	SCASN width negated.		60{}	-	-	
4	SCWTN low to SCDSN asserted.		10{-33}	-	-	
5	SCASN,SCDSN negated to SCWTN high.		10{}	-	-	
6	SCASN,SCDSN negated to DTACKN negated.		0{3}	-	20{10}	

7	WRITE_DATA valid to SCDSN asserted.		10{}	-	-	
8	SCASN,SCDSN negated to WRITE_DATA invaild.		10{1}	-	-	
10	SCASN asserted to SCAVECN,SCIPL[2:0]N valid.		-	-	tC+40{63}	
11	SCASN,SCDSN negated to SCAVECN,SCIPL[2:0]N invalid.		0{8}	-	-	

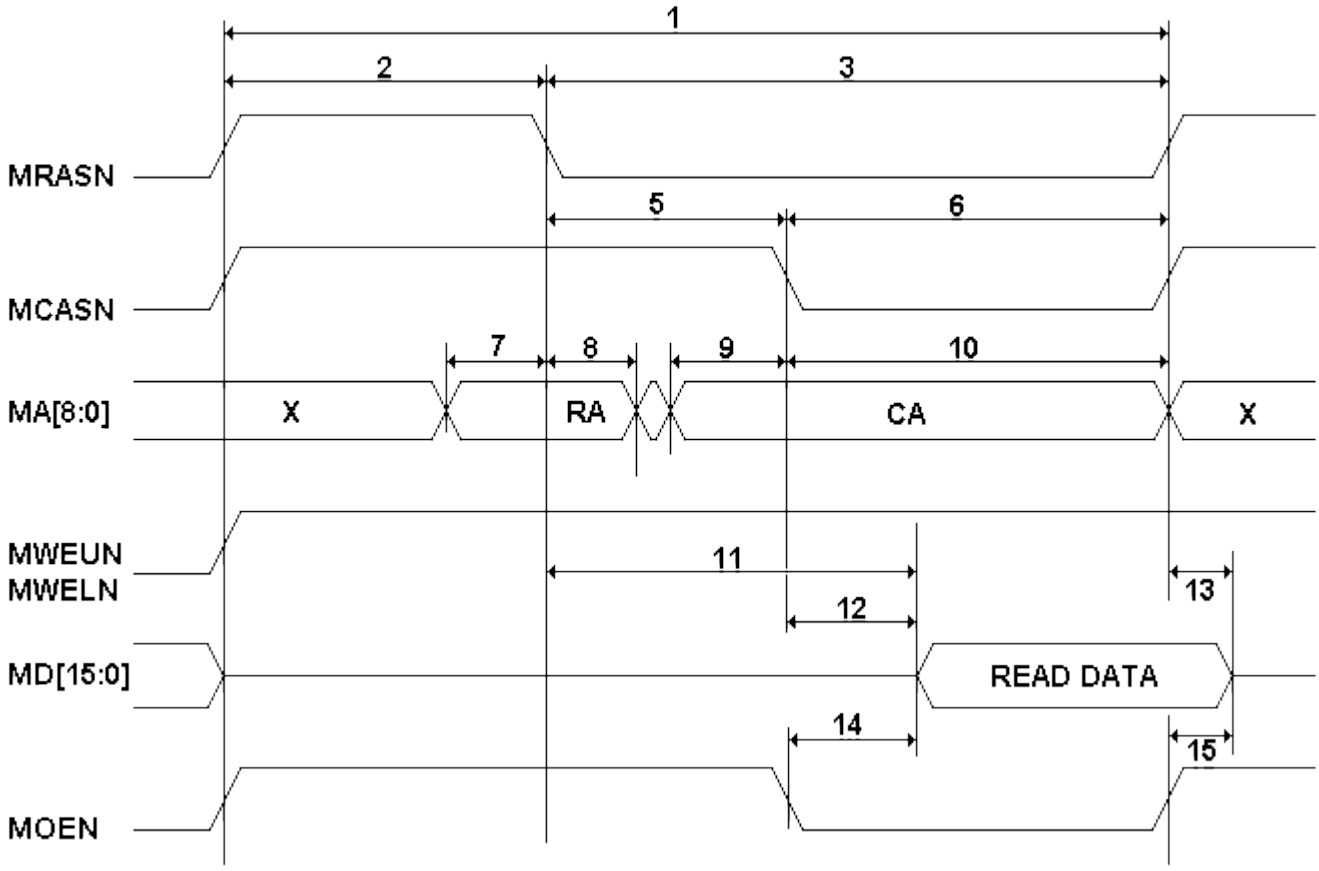


Sound memory interface timing

Sound memory read

No.	Code	Item	Measurement conditions	Minimum	Standard	Maximum	Unit
1	tRC	Random read cycle	CL=30pF	-	4.0tC	-	ns
2	tRP	RASN precharge time		55{65}	1.5tC	-	
3	tRAS	RASN pulse width		90{104}	2.5tC	-	
5	tRCD	RASN and CASN delay time		30{43}	1.0tC	-	
6	tCAS	CASN pulse width		40{60}	1.5tC	-	
7	tASR	Low address setup time		10{58}	1.5tC	-	
8	tRAH	Low address hold time		15{22}	0.5tC	-	
9	tASC	Column address setup time		5{20}	0.5tC	-	
10	tCAH	Column address hold time		30{67}	1.5tC	-	

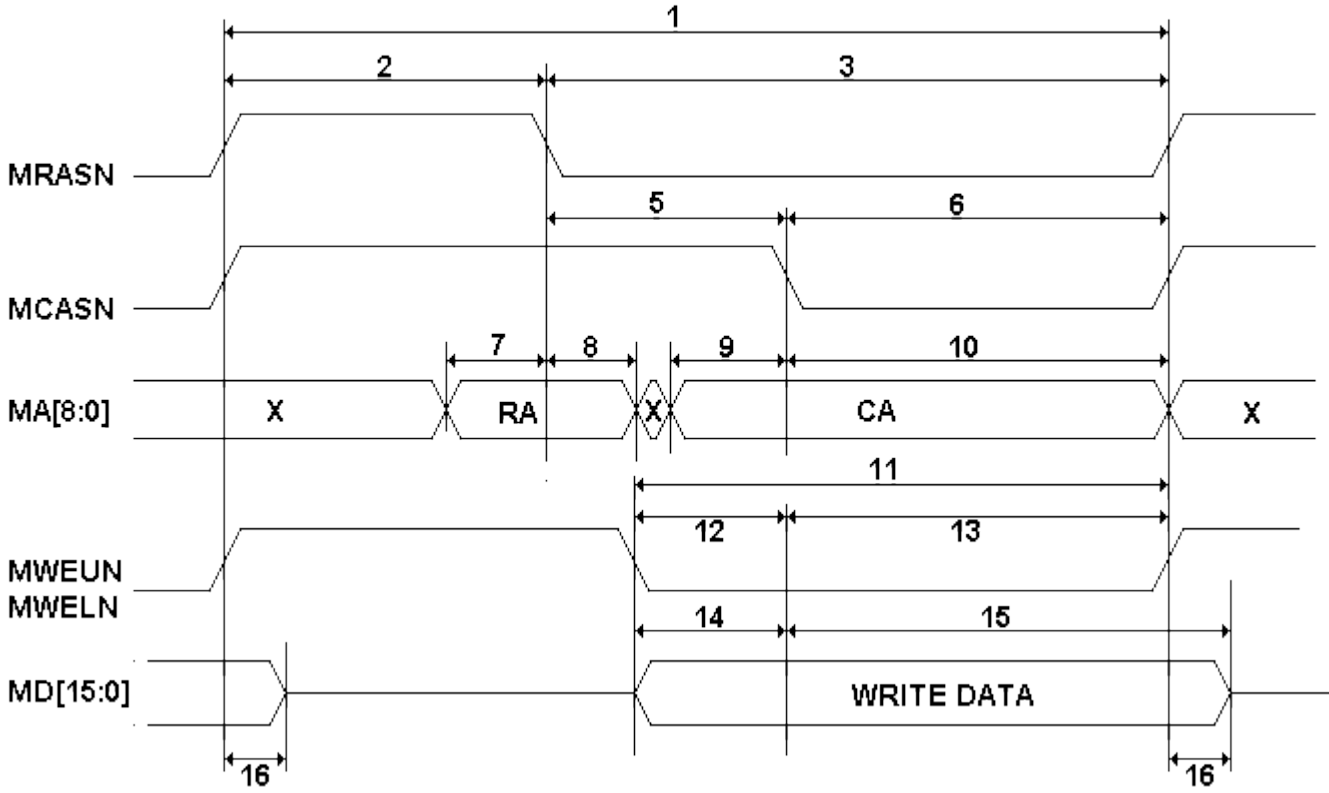
11	tRAC	Low address access time		75{88}	2.0tC+10	-	
12	tCAC	Column address access time		25{44}	1.0tC+10	-	
13	tOH	Output data hold time		0{-11}	-	-	
14	t0EH	Access time from OEN		25{42}	1.0tC+10	-	
15	tOFF	Output data off time		-	-	-	



Sound memory write

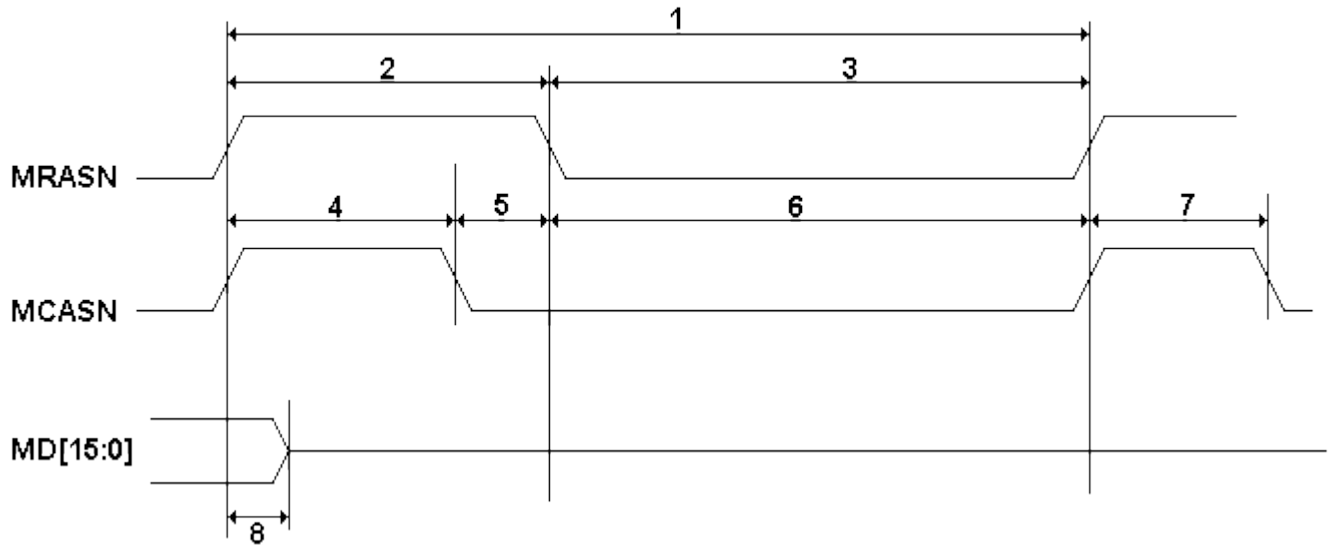
No.	Code	Item	Measurement conditions	Minimum	Standard	Maximum	Unit
1	tRC	Random write cycle	CL=30pF	-	4.0tC	-	ns
2	tRP	RASN precharge time		55{66}	1.5tC	-	
3	tRAS	RASN pulse width		90{104}	2.5tC	-	
5	tRCD	RASN and CASN delay time		30{43}	1.0tC	-	
6	tCAS	CASN pulse width		40{60}	1.5tC	-	
7	tASR	Low address setup time		10{56}	1.5tC	-	
8	tRAH	Low address hold time		15{23}	0.5tC	-	
9	tASC	Column address setup time		5{19}	0.5tC	-	
10	tCAH	Column address hold time		30{66}	1.5tC	-	
11	tWP	Write command pulse width		60{81}	2.0tC	-	
12	tWCS	Write command setup time		10{19}	0.5tC	-	
13	tWCH	Write command hold time		40{59}	1.5tC	-	
14	tDS	Write data setup time		30{43}	1.0tC	-	

15	tDH	Write data hold time		50{72}	1.5tC	-	
16	tOFF	Output turnoff delay time		-	-	30{16}	



Refresh

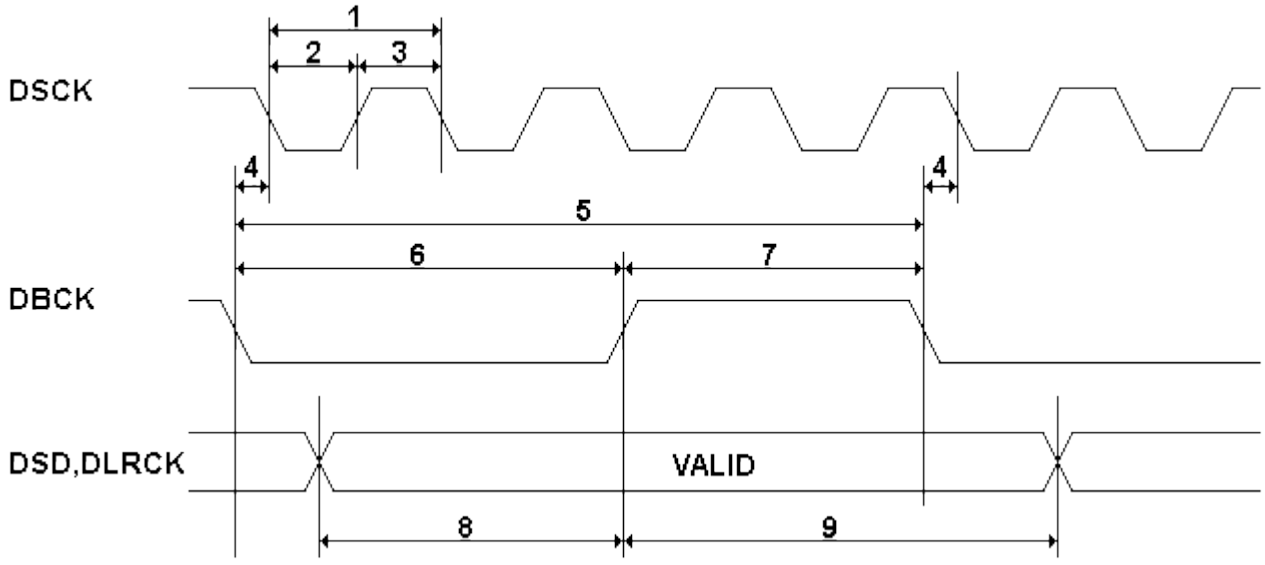
No.	Code	Item	Measurement conditions	Minimum	Standard	Maximum	Unit
1	tRC	Refresh cycle	CL=30pF	-	4.0tC	4.0TC	ns
2	tRP	RASN precharge time		55{65}	1.5tC	-	
3	tRAS	RASN pulse width		90{104}	2.5tC	-	
4	tCPN	CASN precharge time		30{44}	1.0tC	-	
5	tCSR	RASN and CASN setup time		15{21}	0.5tC	-	
6	tCHR	RASN and CASN hold time		90{104}	2.5tC	-	
7	tRPC	Time from RASN precharge to CASN active		30{43}	1.0tC	-	
8	tOFF	Output turnoff delay time		-	-	1.5tC-30	



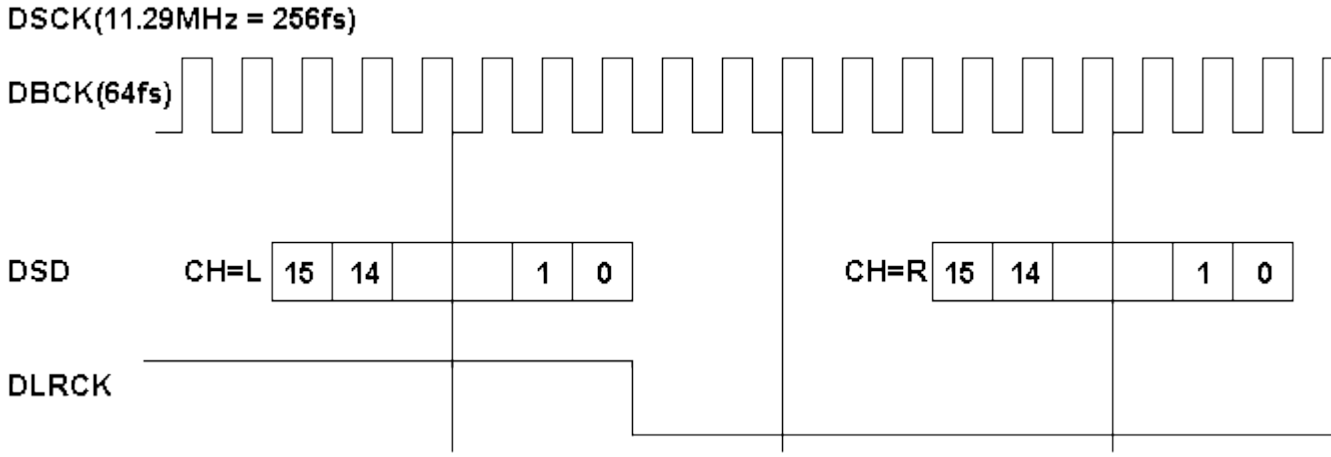
Digital interface

DAC output

No.	Code	Item	Measurement conditions	Minimum	Standard	Maximum	Unit
1	tSC	DSCK cycle time	CL=30pF	-	2.0tC	-	ns
2	tSL	DSCK low time		1.0tC-20	1.0tC	1.0tC+20	
3	tSH	DSCK high time		1.0tC-20	1.0tC	1.0tC+20	
4	tSD	DBCK and DSCK delay time		-20{-3}	0	20{0}	
5	tBC	DBCK cycle time		-	8.0tC	-	
6	tBL	DBCK low time		4.0tC-20	4.0tC	4.0tC+20	
7	tBH	DBCK high time		4.0tC-20	4.0tC	4.0tC+20	
8	tS	Setup time		4.0tC-20	4.0tC	-	
9	tH	Hold time		4.0tC-20	4.0tC	-	

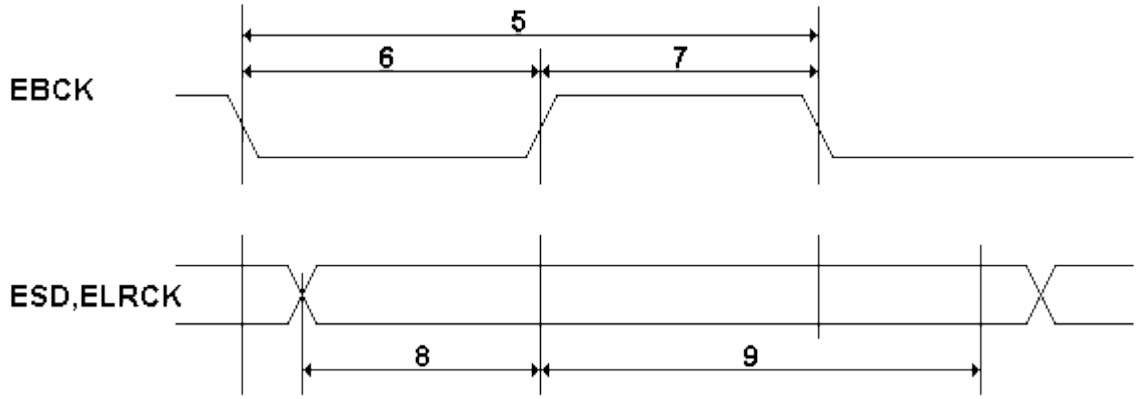


Note:
Interface format (when DAC18B = 0)



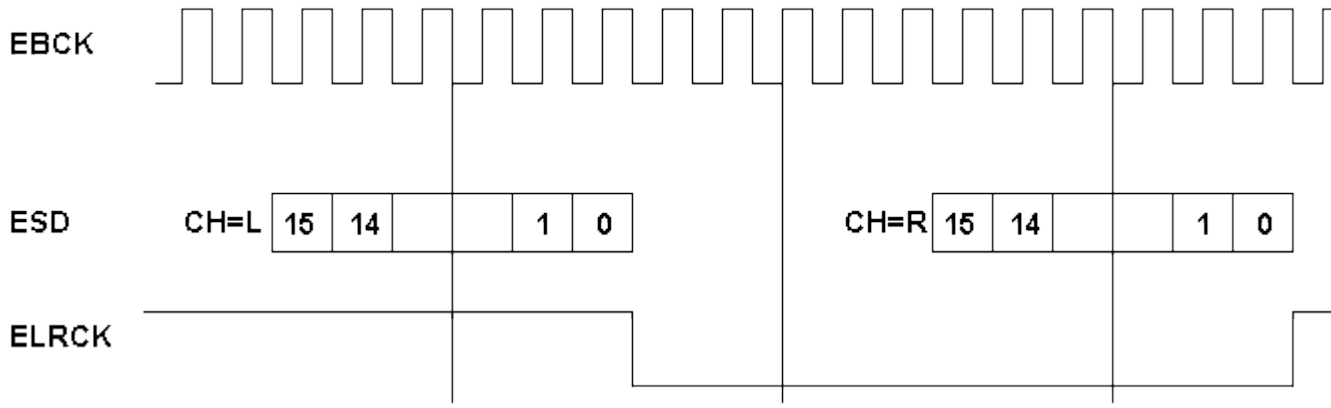
Digital sound input

No.	Code	Item	Measurement conditions	Minimum	Standard	Maximum	Unit
5	tBC	EBCK cycle time		-	8.0tC	-	ns
6	tBL	EBCK low time		100	4.0tC	8.0tC-100	
7	tBH	EBCK high time		100	4.0tC	8.0tC-100	
8	tS	Setup time		20{1}	-	-	
9	tH	Hold time		20{1}	-	-	

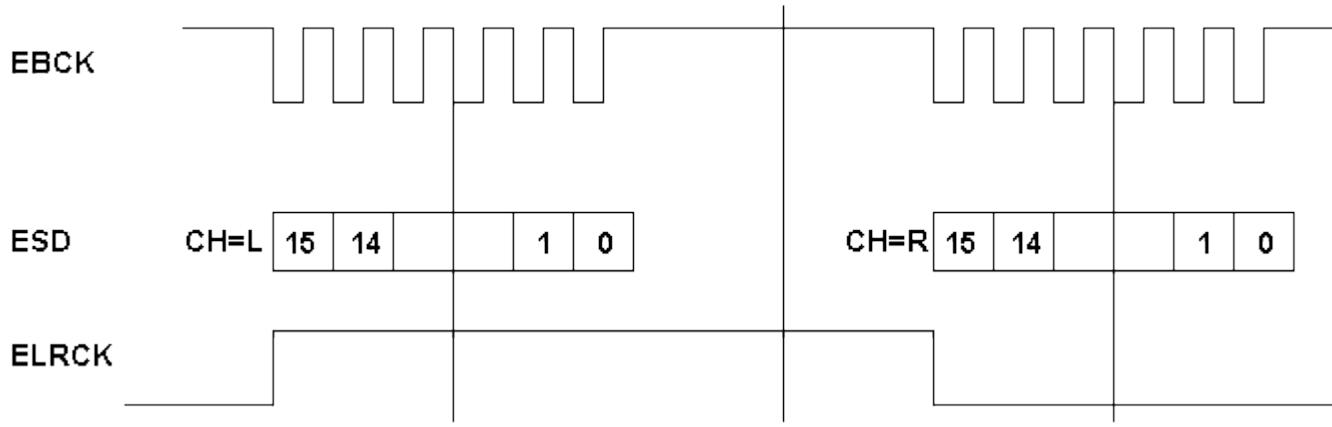


Note:
Interface format

(First: EBCK continuous)



(Second: EBCK noncontinuous)



Note:
Regardless of whether EBCK is continuous or noncontinuous, the transition of ELRCK must occur between the fetch timing for the data of bit 0 (EBCK rise) and the next fetch timing for the data of bit 15 (EBCK rise).

Contents

History of Updates

July 28 1997

- Pin table changed. (MCINTN and MHDQM added.)
- Game port eliminated from overview.
- Channel data Q changed to Q [4:0]. Description of register changed also.
- EFSDL and EFPAN were 18 ch so added.
- Insufficient DMA addresses, so DRGA and DLG changed to [14:1].
- Interrupt registers divided into read and mask registers.
- Both AEG and FEG can now be monitored. Description of EG changed.
- Description of AR, RP, and L [7:0] added.
- M [7:0] (interrupt end register) added. Description of register added.

July 22 1997

- Correction of mistake in text.
- Minor changes to pin table.

Ver. 0.716

- Game port eliminated.
  - RTC, that was in game port data, moved to common data.
  - Game port data eliminated.
  - Pin for game port eliminated.

- Memory changed so that up to 64 Mb can be connected.
  - Addresses of register map changed extensively.
  - SA, RBP, and DMEA expanded to 23 bits.
  - Common data M16MB renamed M8MB.
  - Description of common data M8MB changed.

- One DRAM address added.

- INT [2:0] changed to one, and is now INTN. Hence, the description of the register has been changed.

- Digital input unified.
- Channel data EFSDL and EFPAN changed.
  - DSP data EXTS changed.
  - Description of registers changed.
  - Changes made to DSP.

- G2 bus changed slightly.

Ver. 0.702

- Package overview added to reference manual.
- Pin table changed in accordance with changes to master clock, memory, and G1 bus.
- {insert}. Register map and register description changed.
- Read buffer for game port changed from 1024 to 256 bytes.
- In loop processing description, data readout is ??little-endian??.
- Description of ADPCM added.
- Description of AEG added.
- Description of LFO added.
- Partial mistake in mixer block corrected.
- EG rate calculation table added to FEG.
- Description of DSP added.
- RBP was only 8 Mb maximum; this has been changed to 16 Mb.
- DMEA was only 8 Mb maximum; this has been changed to 16 Mb.

Ver. 0.618

- Bits increased in mixer block so that mixer block can be changed in units of 3 dB. Map has been changed accordingly.
- Monaural mixing register added to common data.
- Details added to mixer block.
- DSP block changed to MADR64.
- Register added for protecting from read operation by main CPU. (ARM access only)
- EFSDL and EFPAN placed in last channel data.
- Registers associated with ARM not decided yet, so left out of description.

Ver. 0.611

- DSP block COEF 128 changed to MADR48.
- Register map changed accordingly.
- Game port read buffer changed to 1 KB.

Ver. 0.XXX

- Sound block changed to 64 ch.
- ADPCM added.
- FEG added.
- Registers streamlined from SCSP.

- RAM changed to 16 Mb maximum.
- Game port added.
- RTC (realtime clock) added.
- Slot information more detailed.
- CPU made ARM.

Channel data

- Time fluctuation filter (FEG) added.
- Q [12:0]
  Resonance data
- FLV0 [12:0]
  Cutoff frequency for attack start time
- FLV1 [12:0]
  Cutoff frequency for attack end time (decay start time)
- FLV2 [12:0]Cutoff frequency for decay end time (sustain start time)
- FLV3 [12:0]
  Cutoff frequency for KOFF time
- FLV4 [12:0]
  Cutoff frequency after release
- FAR [4:0]
  Specifies the rate of transition of FEG in attack status. (Volume transition is increased.)
- FD1R [4:0]
  Specifies the rate of transition of FEG in decay 1 status. (Volume transition is decreased.)
- FD2R [4:0]
  Specifies the rate of transition of FEG in decay 2 status. (Volume transition is decreased.)
- FRR [4:0]
  Specifies the rate of transition of FEG in release status. (Volume transition is decreased.)
- LPCTL [1:0] --> LPCTL
  One bit, because loop has become forward only.
- SSCTL [1:0] --> SSCTL
  Sound input data is PCM and noise only.
- PCM8B --> PCMS [1:0]
  Instead of PCM8B, 16-bit PCM, eight-bit PCM, and four-bit ADPCM are selected with this register.
- OCT [3:0]
  PCM enables -8 through +7 octaves; when ADPCM is set to +1 octave or more, it is limited to +1 octave.
- IMXL [2:0] -->IMXL [3:0]
  Output level can be changed in units of 3 dB instead of 6 dB.
- DISDL [2:0] -->DISDL [3:0]
  Output level can be changed in units of 3 dB instead of 6 dB.
- EFSDL [2:0] -->EFSDL [3:0]
  Output level can be changed in units of 3 dB instead of 6 dB.

Common data

- LP
  Loop end flag
- AEMRST
  ARM reset register
- MEM4MB --> MEM16MB
  Name changed.

- MSLC [4:0] --> MSLC [5:0]
  One bit added to support 64 ch.
- CA [15:12] --> CA [15:10]
  Changed so that buffer progress is monitored each 1 k.
- EG [9:5] -> EG [9:3]
  Changed for more detailed EG control.
- RTC [31:0] (R/W)
  Indicates counter status in increments of one per second. Can count approximately 130 years with 32 bits.
