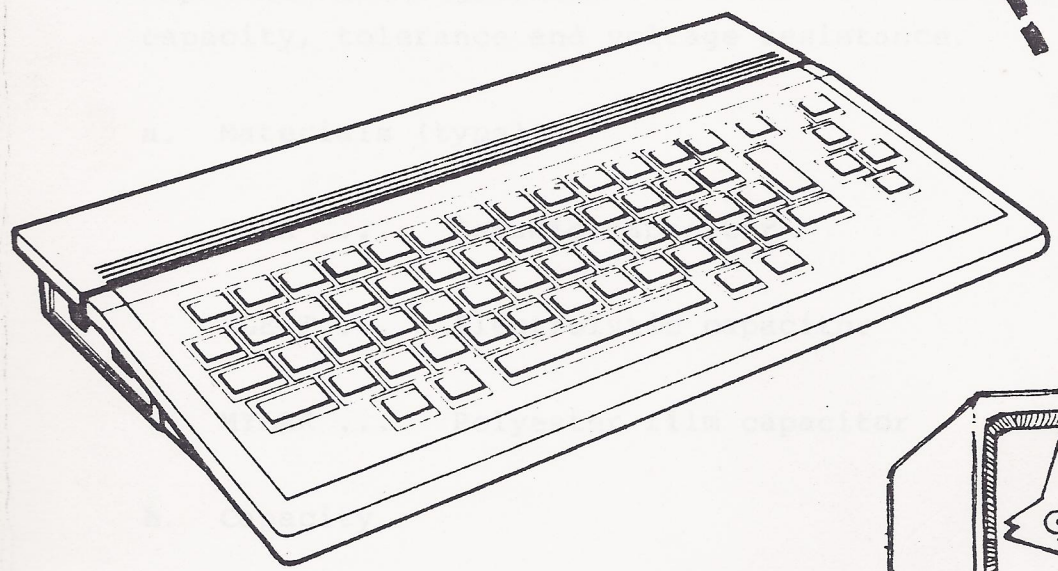
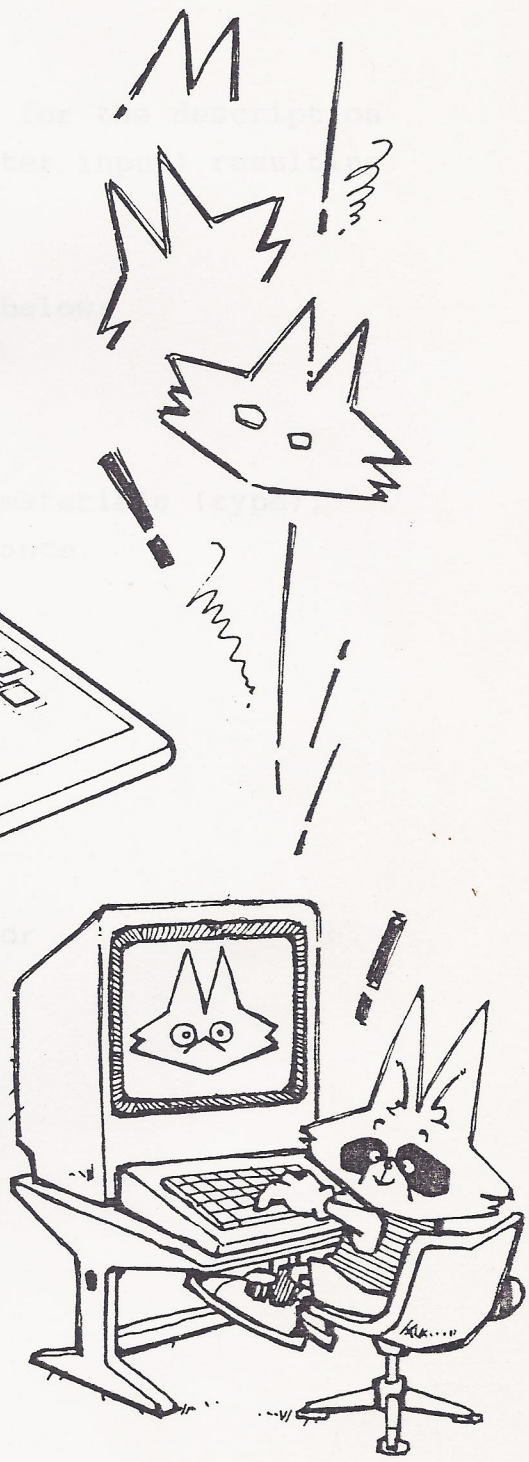
SEGA®

Personal Computer

SC-3000

Service Manual





SEGA ENTERPRISES, LTD.

1. SC-3000 SERVICE MANUAL

2. EXPLANATION OF THE ATTACHED PARTS LIST (ABBREVIATIONS, ETC.)

In the attached parts list, the column for the description of parts has limited digits (for computer input) resulting in some insufficient expressions.

The main abbreviations used are given below:

① Capacitor

Expressions are given in the order of materials (type), capacity, tolerance and voltage resistance.

a. Materials (type)

CERA ..... Ceramic capacitor

ELECT .... Electrolytic capacitor

MYLAR .... Polyester film capacitor

b. Capacity

0.1 U = 0.1μ F 470P = 470pF

c. Tolerance

J = ±10% K = ±5% Z = $^{+80}_{-20}$ %, M = ±20%

② Resistance

Expressions are given in the order of material (type), resistance (Ω), tolerance and allowable output.

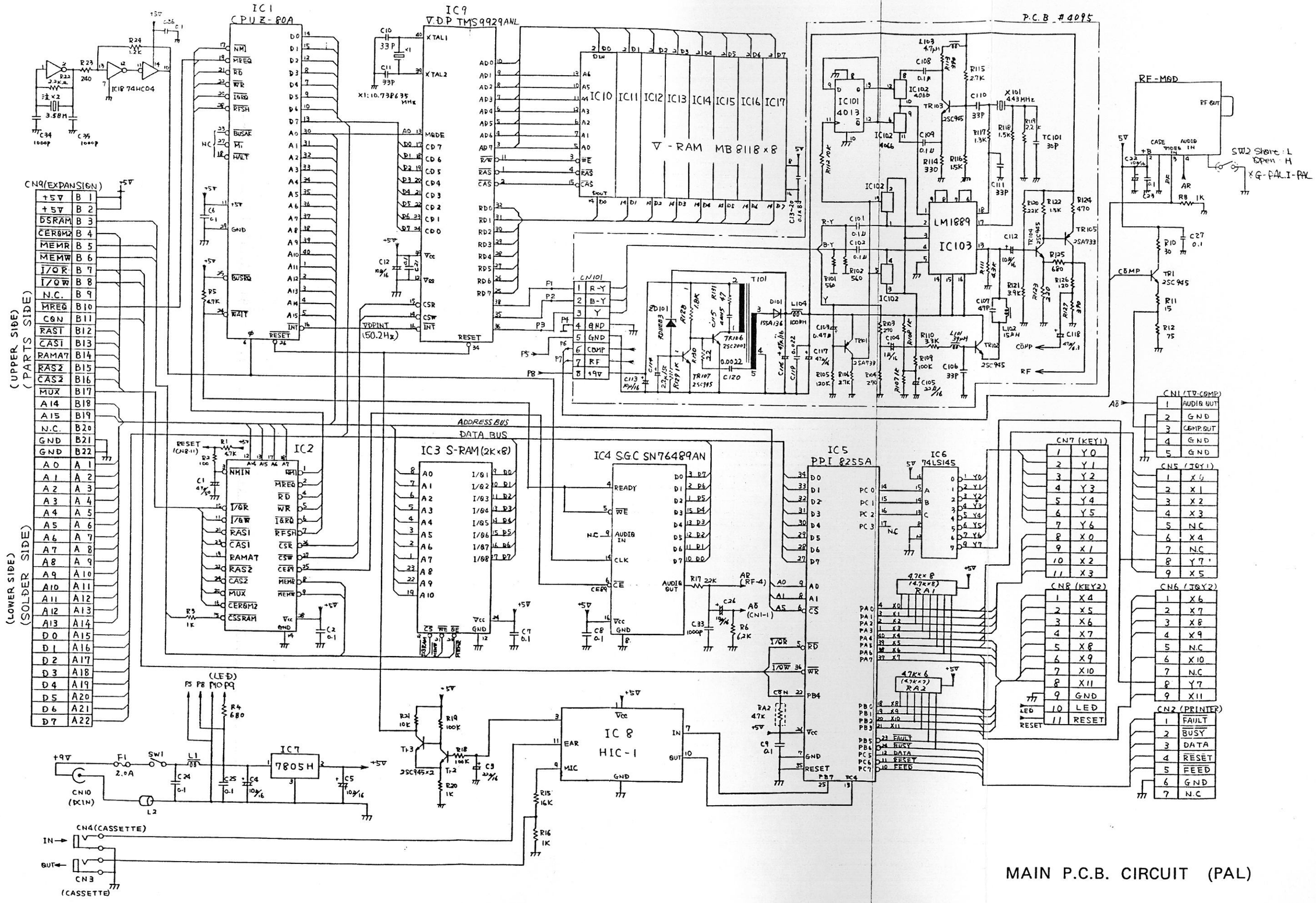
Example: CARBON R H IK J 1/4W
(Resistor) (Horizontal)
(V ... Vertical)

③ Others

TR ..... Transistor
D ..... Diode
V ..... Variable Resistor
SEMI VR ..... Semi-fixed resistor

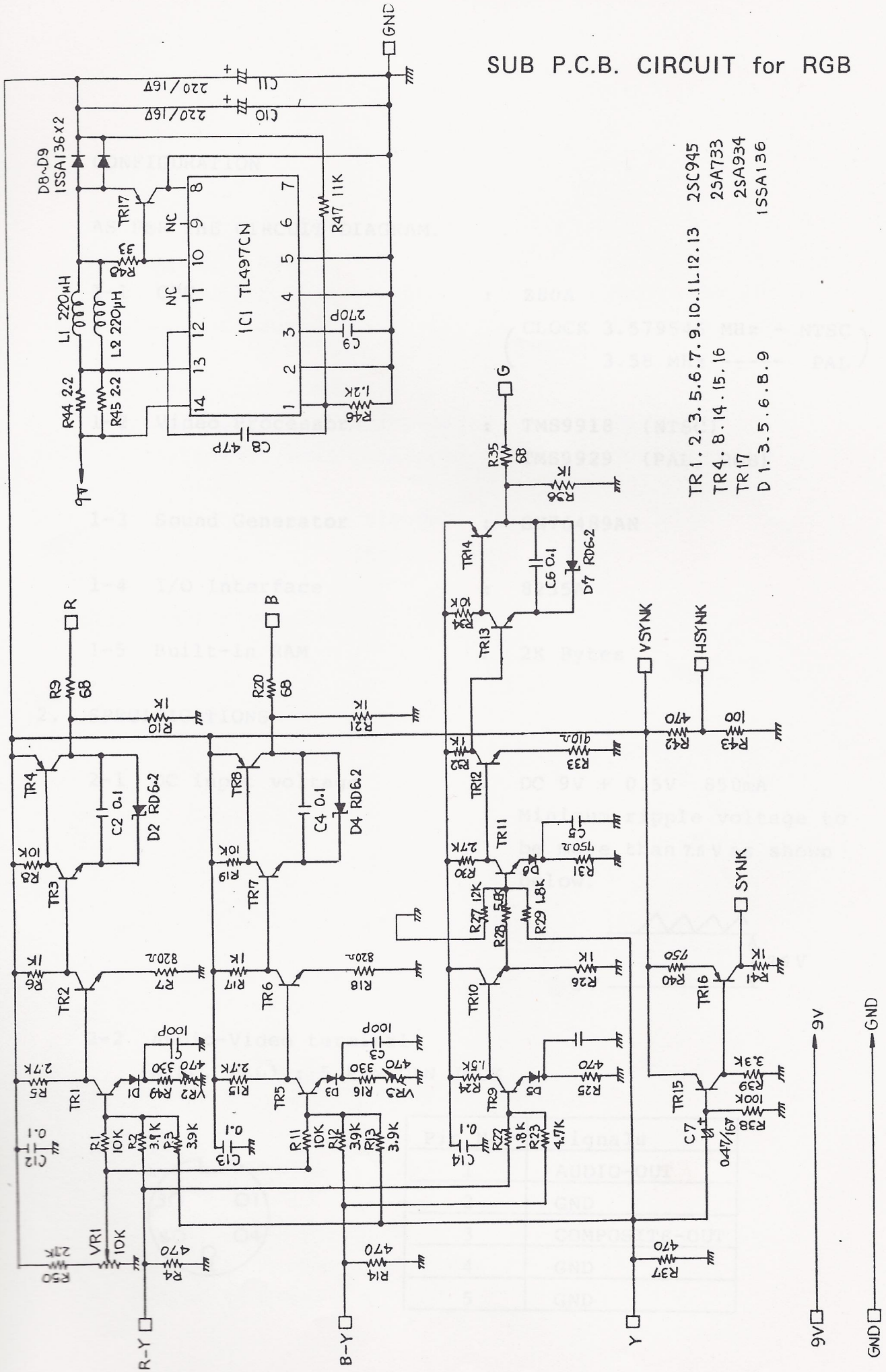
SC-3000 SERVICE MANUAL

- CONTENTS -



MAIN P.C.B. CIRCUIT (PAL)

SUB P.C.B. CIRCUIT for RGB



1. CONFIGURATION

AS PER THE CIRCUIT DIAGRAM.

1-1 CPU : Z80A
(CLOCK 3.579545 MHz - NTSC
3.58 MHz ----- PAL)

1-2 Video Processor : TMS9918 (NTSC)
TMS9929 (PAL, RGB)

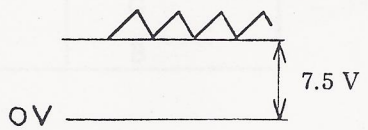
1-3 Sound Generator : SN76489AN

1-4 I/O Interface : 8255A

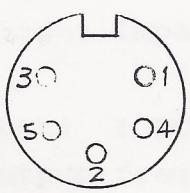
1-5 Built-in RAM : 2K Bytes

2. SPECIFICATIONS

2-1 DC input voltage : DC 9V + 0.5V 850mA
Minimum ripple voltage to be more than 7.5 V as shown below.



2-2 Audio-Video terminal
(NTSC, PAL) : 5 PIN DIN JACK



Pin No.	Signals
1	AUDIO-OUT
2	GND
3	COMPOSITE-OUT
4	GND
5	GND

2-2-1 AUDIO - OUT

Allowable load impedance : More than 10KΩ

Output level : 1V max + 0.2V

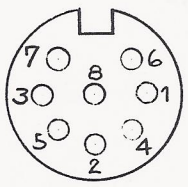
2-2-2 COMPOSITE - OUT

Recommended load impedance : 75Ω

Allowable load impedance : More than 70

Output level : 0.9VP-P ± 0.1 V
(White level)

(RGB) : 8 PIN DIN JACK



(côté micro)
femelle

PIN NO.	SIGNALS
1	AUDIO
2	GND
3	$\overline{\text{SYNK}}$
4	HSYNK
5	VSYNK
6	R
7	G
8	B

2-3 Video RF terminal

(NTSC) : RCA pin jack

Output frequency : JIS Channel 1 (L-CH)
Channel 2 (H-CH)

Output Impedance : 75Ω

(PAL) : RCA pin jack

Output frequency : Table 1

Output impedance : 75 Ω

Table 1

TYPE	Output frequency	Voice Frequency
G-PAL	CCIR 36CH (591.25 MHz)	+5.5 MHz
I-PAL	CCIR 36CH (591.25 MHz)	+6.0 MHz
B-PAL (Australia)	Australia 3CH (86.25 MHz)	+5.5 MHz
	Australia 4CH (95.25 MHz)	+5.5 MHz
B-PAL (New Zealand)	New Zealand 2CH (55.25 MHz)	+5.5 MHz
	New Zealand 3CH (62.25 MHz)	+5.5 MHz
B-PAL (Southeast Asia)	CCIR 3CH (55.25 MHz)	+5.5 MHz
	4CH (62.25 MHz)	+5.5 MHz

2-4 Cassette interface terminal: 3.5φ 2P mini-jack

Output level: 20mV P-P ± 5mV

Input level : More than 1Vp-p

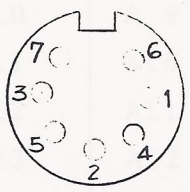
I/O form : As per ROM pack software

Optimum form : L=1200 Hz

H=2400 Hz

1200 baud

2-5 Printer interface : 7 PIN DIN jack



Pin No.	Connection	Signals as per SC-3000 BASIC
1	8255 PB5	$\overline{\text{FAULT}}$
2	8255 PB6	$\overline{\text{BUSY}}$
3	8255 PC5	DATA
4	8255 PC6	$\overline{\text{RESET}}$
5	8255 PC7	$\overline{\text{FEED}}$
6	GND	GND
7	NC	NC

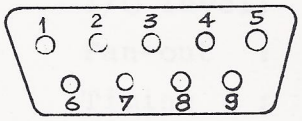
I/O level : TTL

FAN-OUT : *1 TTL

I/O form : Serial (As per ROM pack)

*(Note: this is 1 and not I)

2-6 JOYSTICK



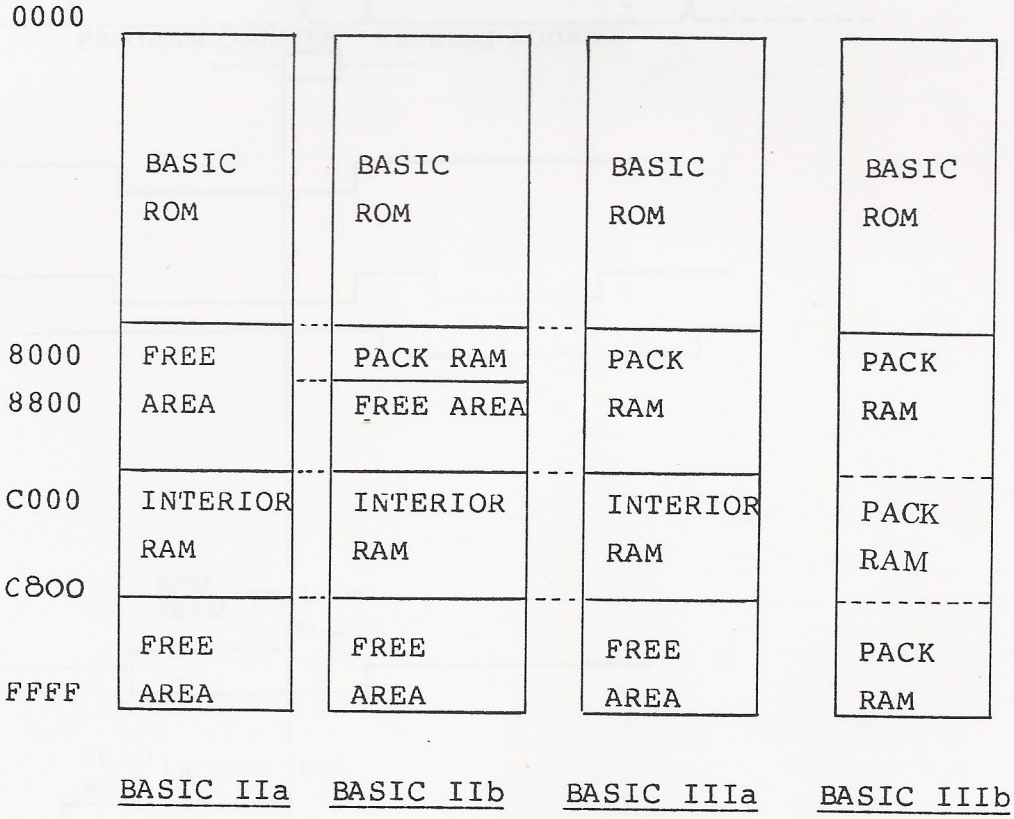
Pin No.	Connection	Pin No.	Connection
1	XO	6	X4
2	X1	7	NC
3	X2	8	Y7
4	X3	9	X5
5	NC		

2-7 ROM/RAM Cartridge slot

Pin No.	Signal	Pin No.	Signal
A 1	A 0 (ADDRESS 0)	B 1	+ 5V
A 2	A 1 (" 1)	B 2	+ 5V
A 3	A 2 (" 2)	B 3	$\overline{\text{DSRAM}}$
A 4	A 3 (" 3)	B 4	$\overline{\text{CEROM2}}$
A 5	A 4 (" 4)	B 5	$\overline{\text{MEMR}}$
A 6	A 5 (" 5)	B 6	$\overline{\text{MEMW}}$
A 7	A 6 (" 6)	B 7	$\overline{\text{I/OR}}$
A 8	A 7 (" 7)	B 8	$\overline{\text{I/OW}}$
A 9	A 8 (" 8)	B 9	NC
A10	A 9 (" 9)	B10	$\overline{\text{MREQ}}$
A11	A10 (" 10)	B11	CON
A12	A11 (" 11)	B12	$\overline{\text{RAS1}}$
A13	A12 (" 12)	B13	$\overline{\text{CAS1}}$
A14	A13 (" 13)	B14	RAMA7
A15	D 0 (DATA 0)	B15	$\overline{\text{RAS2}}$
A16	D 1 (" 1)	B16	$\overline{\text{CAS2}}$
A17	D 2 (" 2)	B17	$\overline{\text{MUX}}$
A18	D 3 (" 3)	B18	A14
A19	D 4 (" 4)	B19	A15
A20	D 5 (" 5)	B20	NC
A21	D 6 (" 6)	B21	GND
A22	D 7 (" 7)	B22	GND

I/O level: TTL
Fan-out : 1TTL
Timing : As per Fig. 2-1～2-3.

2-8 Memory map

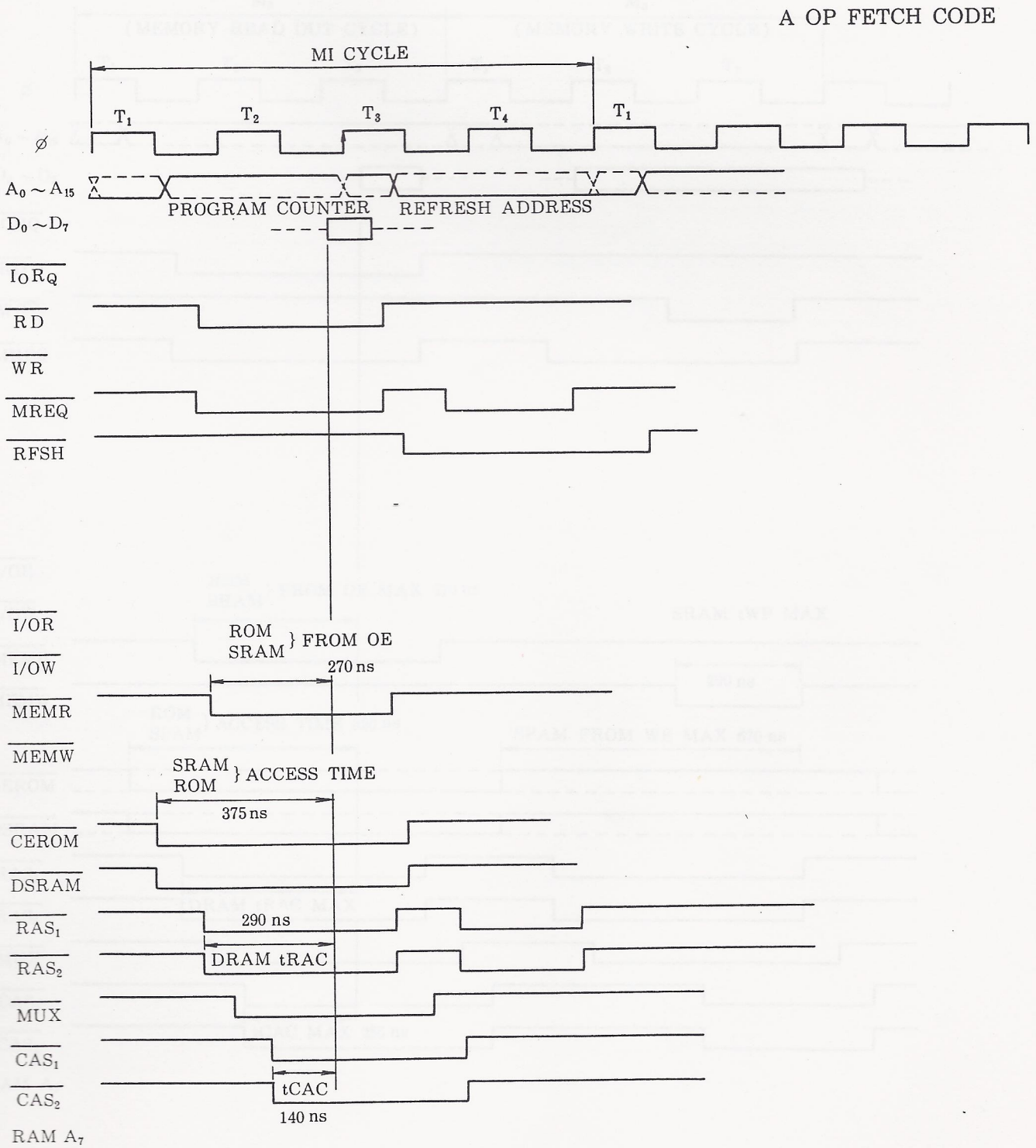


2-9 I/O MAP

	7	6	5	4	3	2	1	0
SN76489 (SOUND)	$\overline{CS}$	X	X	X	X	X	X	X
TMS9918* (VDP)	X	$\overline{CS}$	X	X	X	X	X	MODE
8255A (I/O)	X	X	$\overline{CS}$	X	X	X	MODE	
RESERVED	X	X	X	$\overline{CS}$	$\overline{CS}$	$\overline{CS}$	X	X

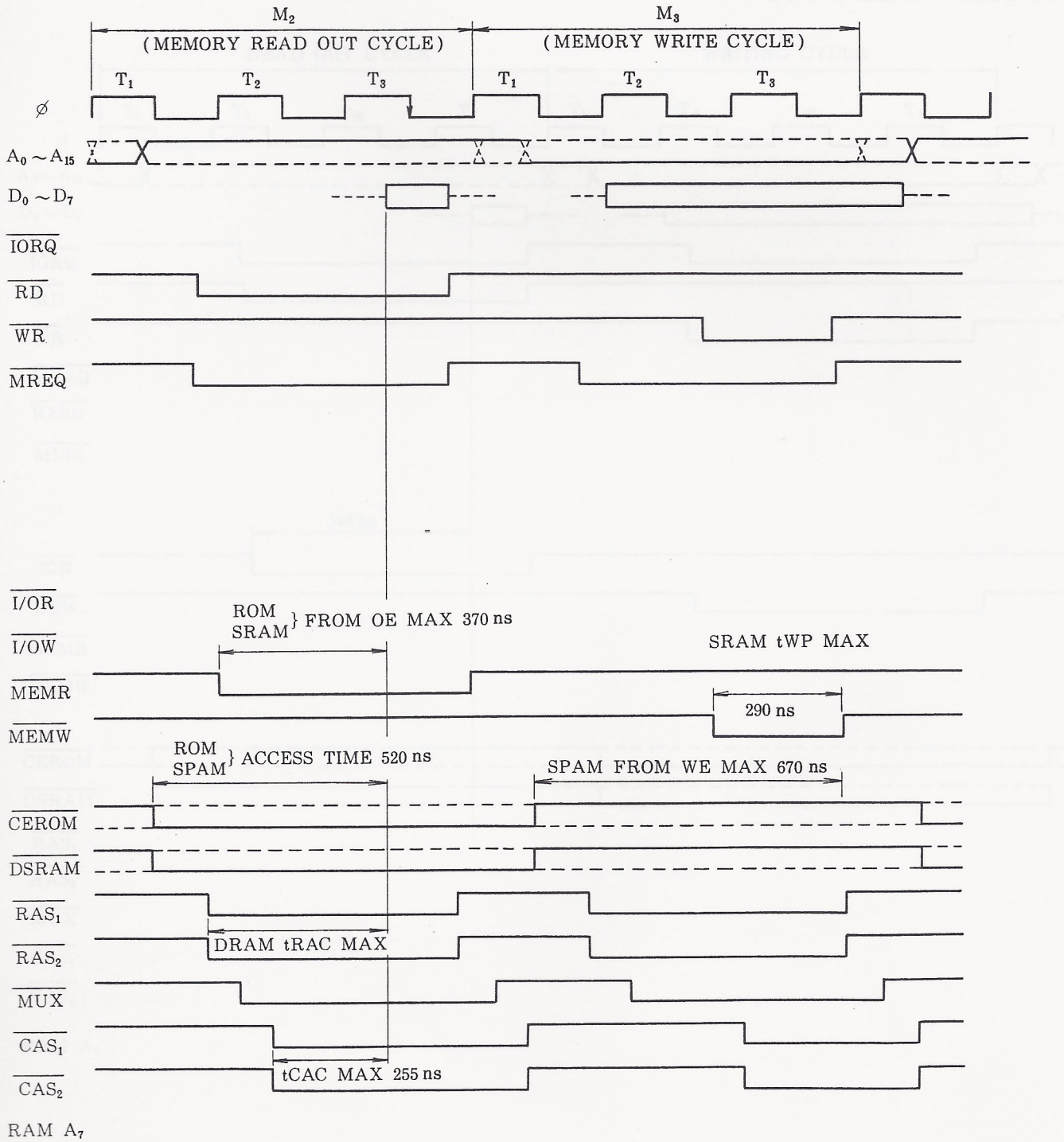
* TMS9929 applies to PAL and RGB.

CARTRIDGE TIMING CHART (1/3)
(10ns / mm)



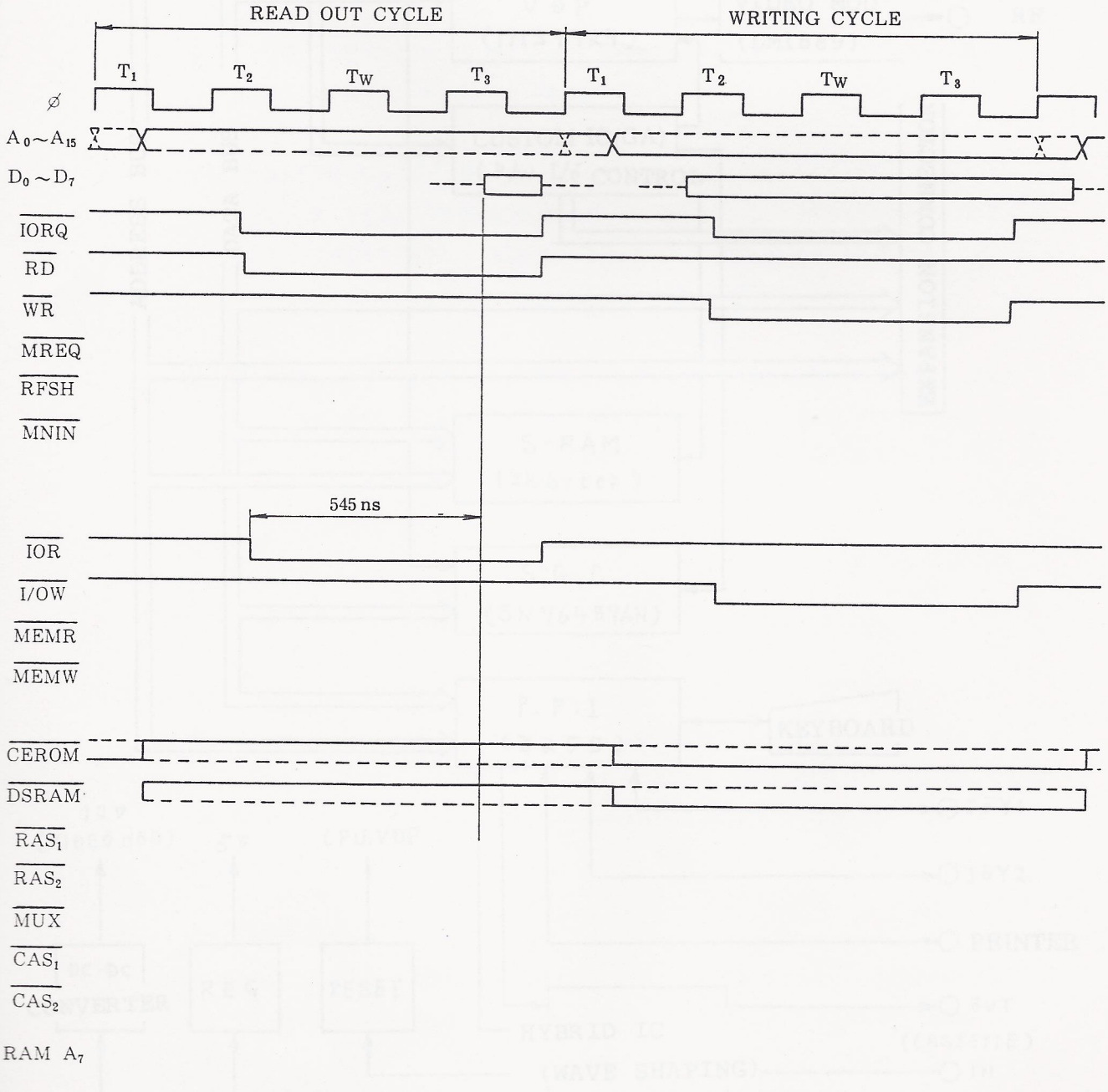
CARTRIDGE TIMING CHART (2/3)
(10ns / mm)

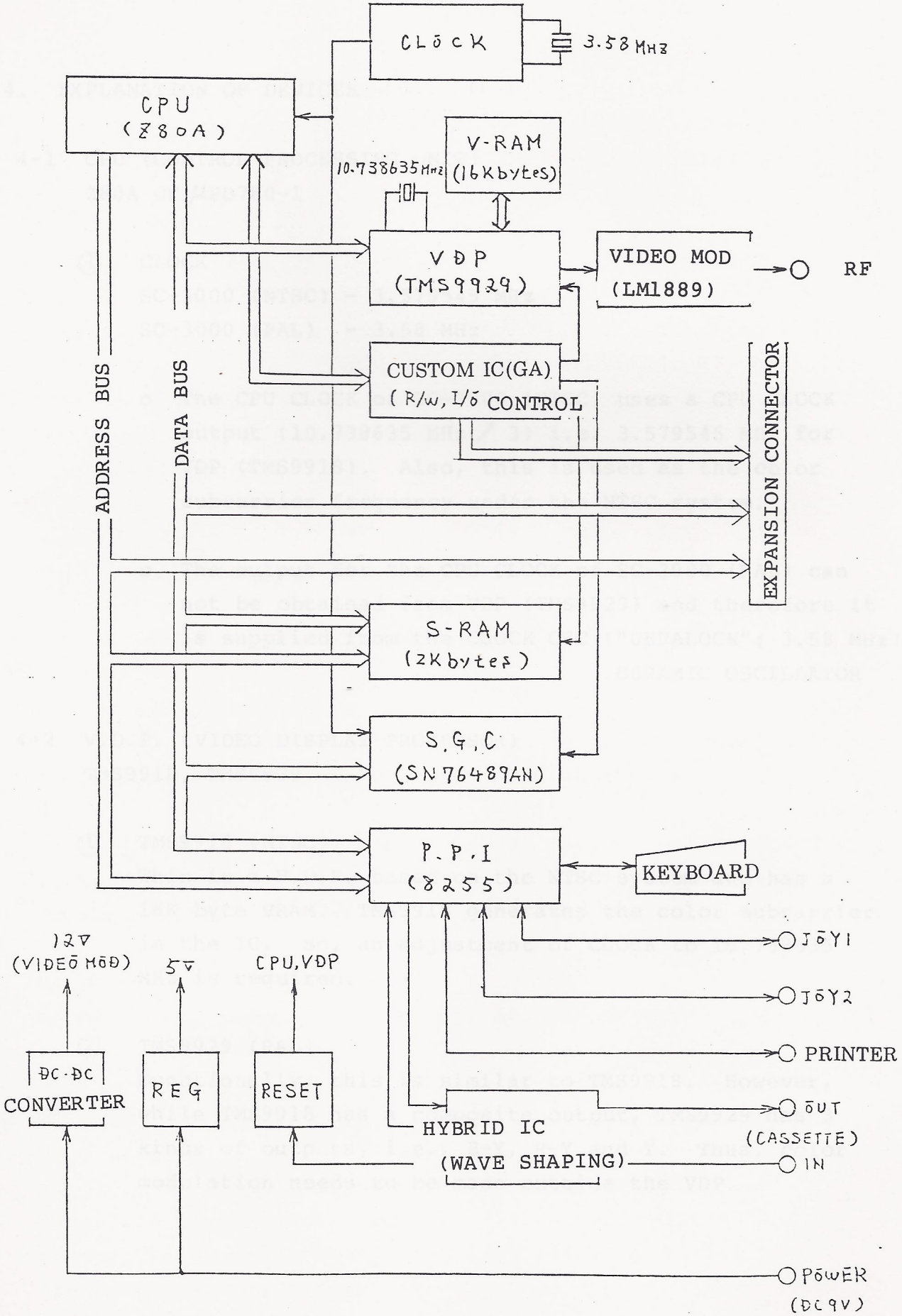
B. MEMORY READ－OUT/WRITE CYCLE



CARTRIDGE TIMING CHART (3/3)
(10 ns / mm)

C : I/O READ/WRITE CYCLE





(Fig. 3-2) SC-3000 (PAL) BLOCK DIAGRAM

4. EXPLANATION OF DEVICES

4-1 CPU (CONTROL PROCESSING UNIT)

Z80A or μPD780-1

① CLOCK

SC-3000 (NTSC) - 3.579545 MHz

SC-3000 (PAL) - 3.58 MHz

- o The CPU CLOCK of SC-3000 (NTSC) uses a CPU CLOCK output (10.738635 MHz / 3) i.e. 3.579545 MHz for VDP (TMS9918). Also, this is used as the color subcarrier frequency under the NTSC system.

- o The output for the CPU CLOCK of SC-3000 (PAL) can not be obtained from VDP (TMS9929) and therefore it is supplied from the CLOCK OSC ("CERALOCK": 3.58 MHz)

CERAMIC OSCILLATOR

4-2 V.D.P. (VIDEO DISPLAY PROCESSOR)

TMS9918, TMS9929

① TMS9918 (NTSC)

This is a V.D.P. based on the NTSC system and has a 16K byte VRAM. TMS9918 generates the color subcarrier in the IC. So, an adjustment of CLOCK to 10.738635 MHz is required.

② TMS9929 (PAL)

Functionally, this is similar to TMS9918. However, while TMS9918 has a composite output, TMS9929 has 3 kinds of outputs, i.e., B-Y, R-Y and Y. Thus, color modulation needs to be made outside the VDP.

Also, in the case of 9929, the subcarrier is not generated in the IC. So, CLOCK frequency adjustments are not necessary.

4-3 CUSTOM IC (gate array)

This has functions to prevent RESET signal chattering and from CPU signal ($\overline{MREQ}$, $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$, $\overline{RFSH}$, A6, A7, A14, A15) to generate CS (chip select) signals of S-RAM, SGC and VDP as well as to generate control signals of exterior ROM and exterior D-RAM.

4-4 S-RAM

This has a memory of 2K bytes (2K x 8 bit).

4-5 S.G.C. (SOUND GENERATION CONTROLLER)

SN76489

IC for sound generation

4-6 P.P.I. (PROGRAMMABLE PERIPHERAL INTERFACE)

8255

This is the IC for the interface and carries out keyboard scanning, joystick scanning, printer signal control and cassette signal control.

4-7 KEYBOARD

Refer to the separate key matrix drawing (Fig. 4)

4-8 Hybrid IC

This is the hybrid IC which carries out cassette signal wave shaping. This IC has an attenuator of 20 dB for output. For input, signals from the cassette tape are shaped to square waves. At the following levels and corresponding frequencies, the 1200 bit/sec. signal is transmitted: 0:1200 Hz

1:2400 Hz

4-9 RESET CIRCUIT

This resets the CPU and VDP when the power is turned ON.

4-10 REGULATOR

This is operated by the logical circuit of 5V stabilized (7805H) power source only (except for PAL).

4-11 VIDEO MODULATOR circuit

The VDP (TMS9929) under the PAL system has no VIDEO composite output and instead, color difference signals of 3 kinds, i.e., the Y, R-Y and B-Y are output. In this circuit, PAL composite video signals are converted from the signals of Y, R-Y and B-Y, and also, amplification of 6 dB (approximately) is carried out as the signal output of LM1889 is insufficient.

4-12 DC-DC converter circuit (PAL)

This circuit is used as the DC-DC converter (PAL) of 9V-12V became necessary due to the specified power source voltage range of 12V for the IC LM1889 used for VIDEO MOD converter circuit.

4-14 RF MOD

The RF MODULATOR has 2 systems, i.e., the NTSC and the PAL, as specified below.

fp: Image frequency
fs: Sound frequency

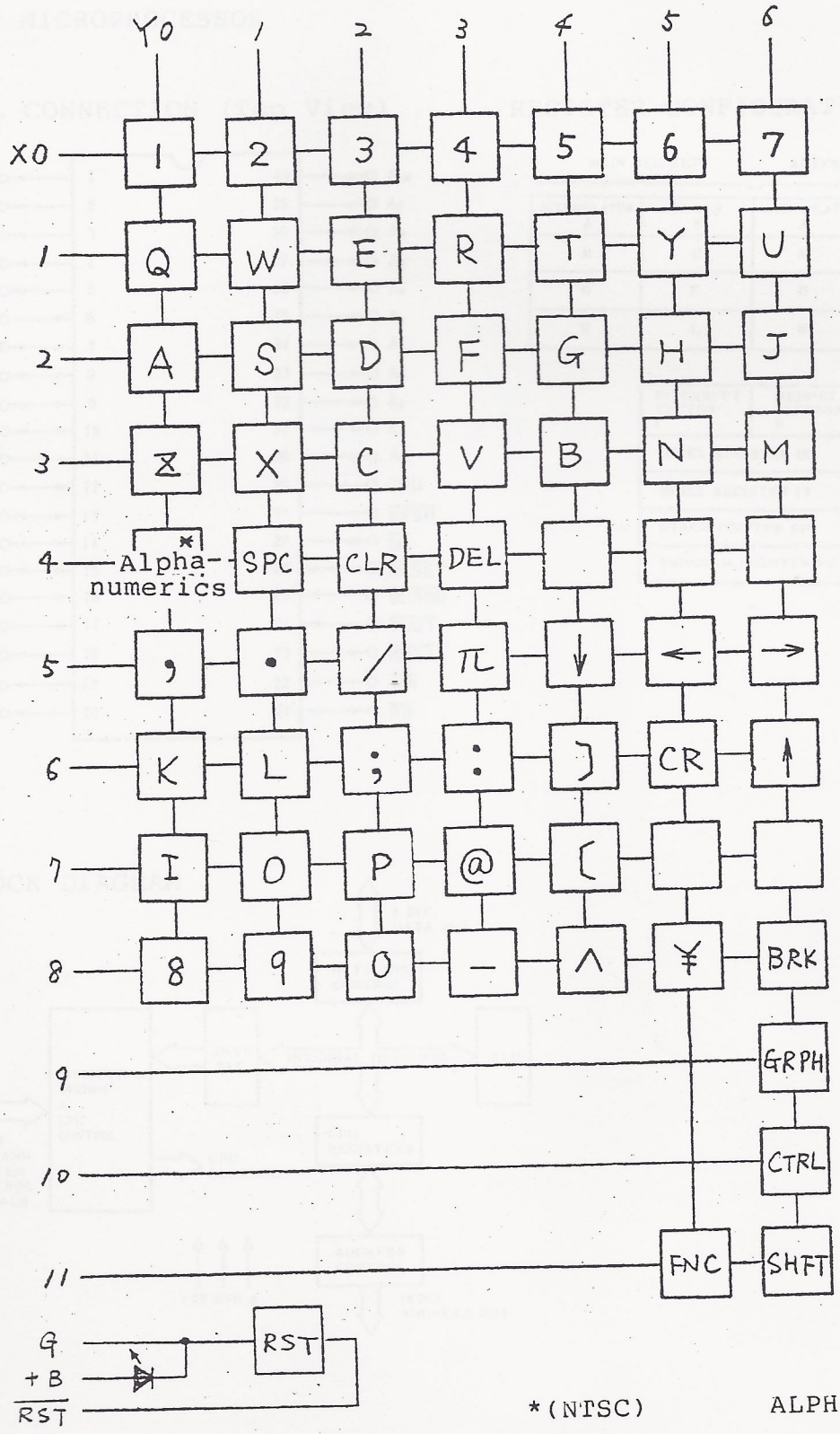
o NTSC

		Channel	fp	fs - fp	Scanning lines
1.	VHF	CH 1	91.25 MHz	44.5 MHz	525 lines
		CH 2	97.25 MHz	44.5 MHz	525 lines

o PAL

UHF	1.	G-PAL CCIR	36 CH	591.25 MHz + 5.5 MHz	625 lines
	2.	I-PAL CCIR	36 CH	591.25 MHz + 6.0 MHz	625 lines
VHF	3.	B-PAL	3 CH	86.25 MHz + 5.5 MHz	625 lines
		(AUSTRALIA)	4 CH	95.25 MHz + 5.5 MHz	625 lines
	4.	B-PAL	2 CH	55.25 MHz + 5.5 MHz	625 lines
		(New Zealand)	3 CH	62.25 MHz + 5.5 MHz	625 lines
	5.	B-PAL	3 CH	55.25 MHz + 5.5 MHz	625 lines
		(Southwest Asia)	4 CH	62.25 MHz + 5.5 MHz	625 lines

(Fig. 4) SC-3000 KEY MATRIX



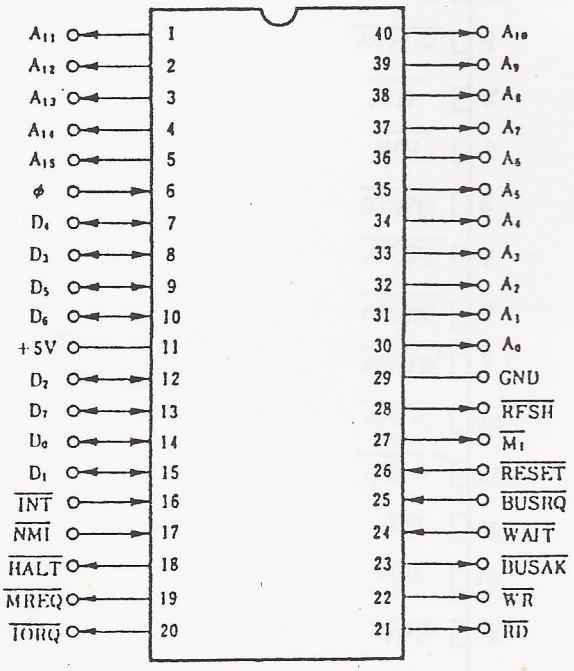
*(NTSC) ALPHANUMERICS
(PAL • RGB) ENG DIER'S

5. IC TERMINAL CONNECTION (INTERIOR BLOCK DIAGRAM)

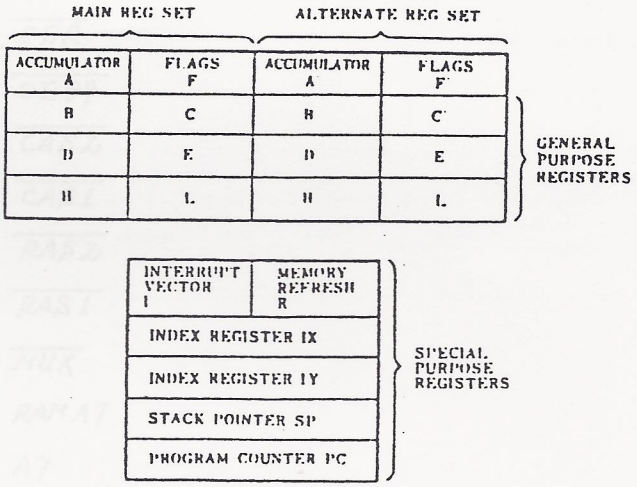
(1) ICI: μPD780 (Z80A)

8 BIT MICROPROCESSOR

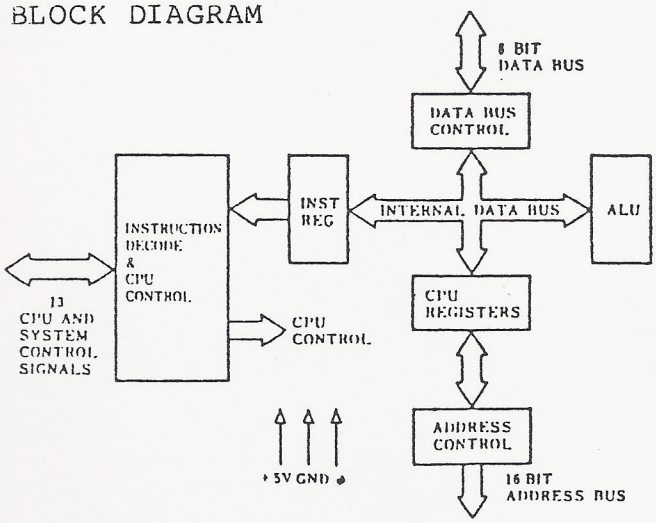
TERMINAL CONNECTION (Top View)



REGISTER CONFIGURATION

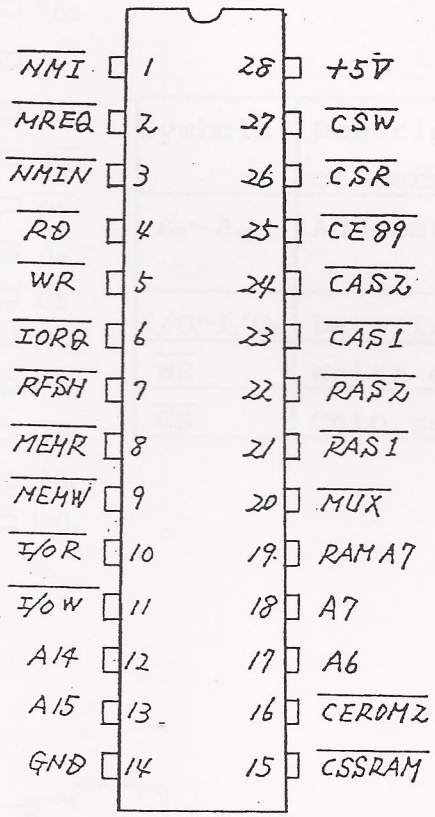


BLOCK DIAGRAM



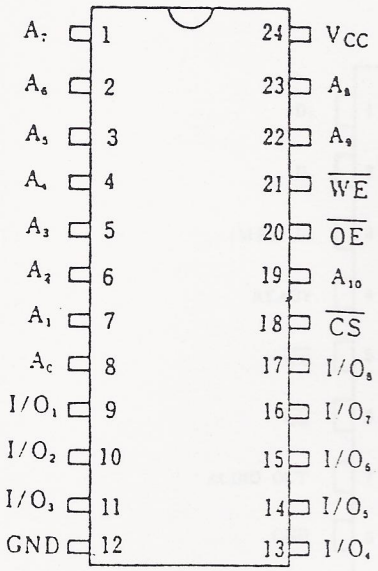
(2) IC2: GATE ARRAY

Terminal connection (Top View)



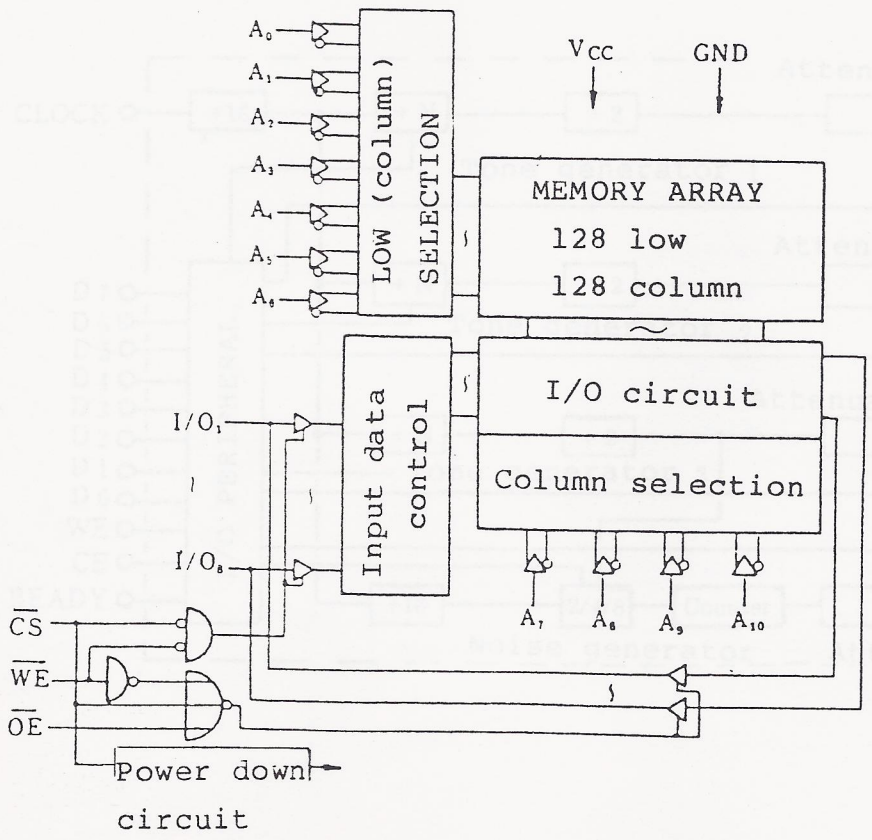
(3) IC3: 2Kx8 S-RAM

Terminal layout (TOP VIEW)



Symbols	Description of terminal	Symbols	Description of terminal
$A_0 \sim A_{10}$	Address input	$\overline{OE}$	Output enable
$I/O_1 \sim I/O_8$	Data I/O	Vcc	Power (+5V)
$\overline{WE}$	Write enable	GND	GND
$\overline{CS}$	Chip select		

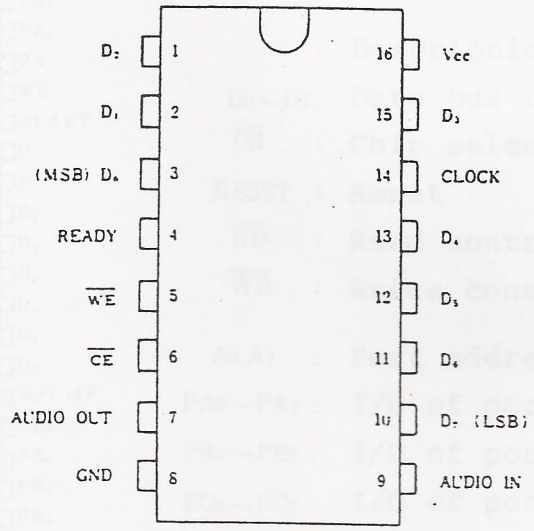
BLOCK DIAGRAM



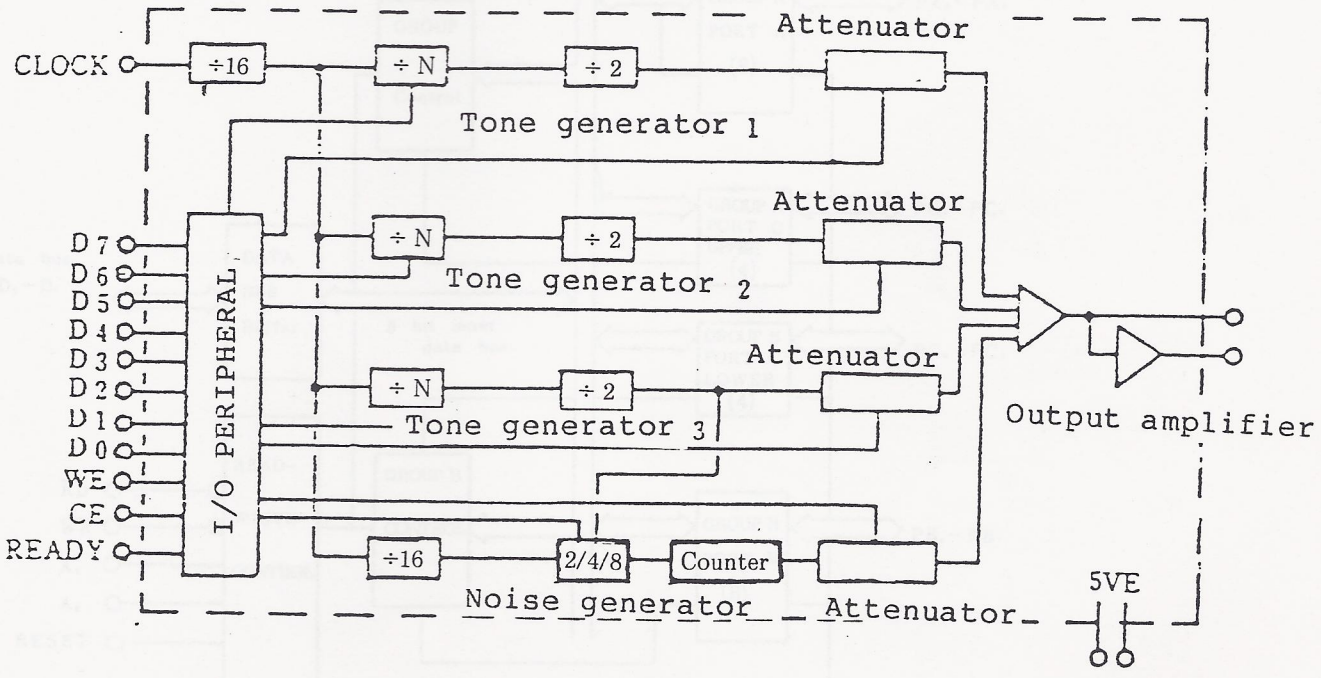
(4) IC4: SN76489AN

SOUND GENERATION CONTROLLER

TERMINAL CONNECTION (Top View)

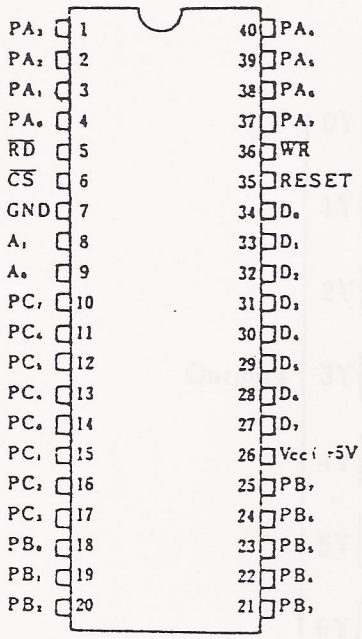


BLOCK diagram



(5) IC5: 8255A

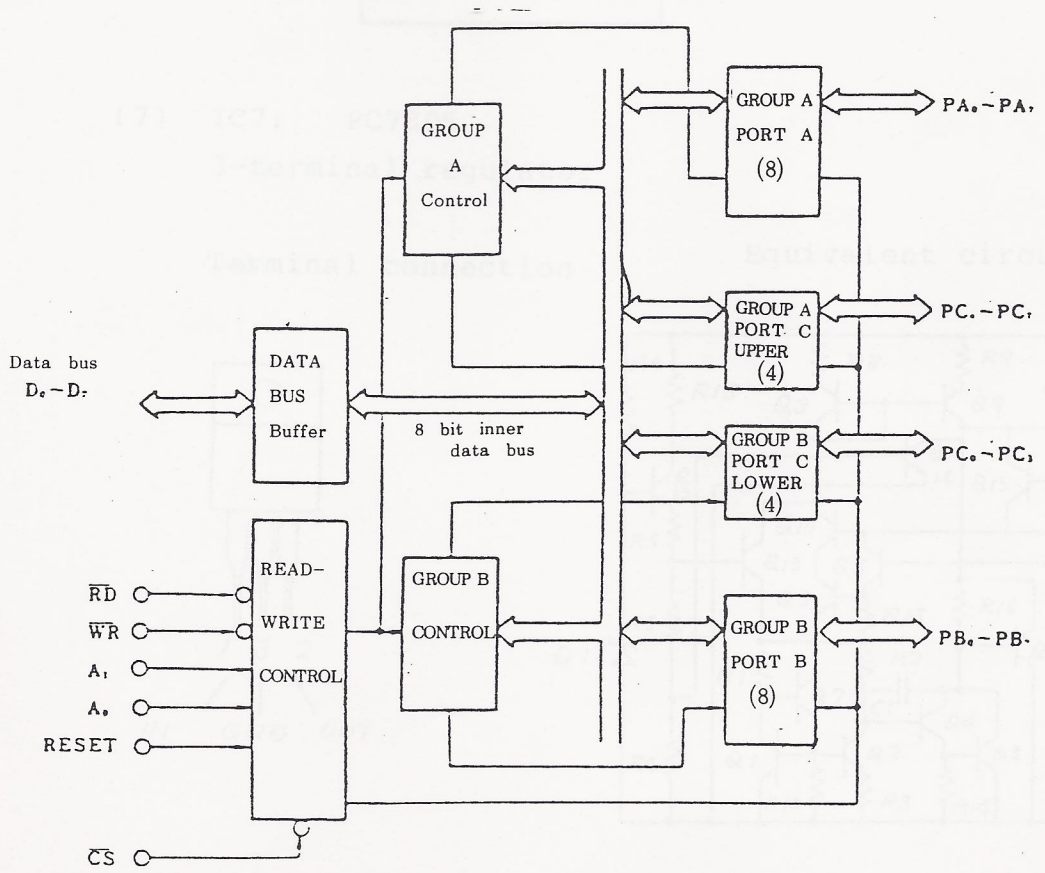
Terminal connection (Top View)



Description of terminals

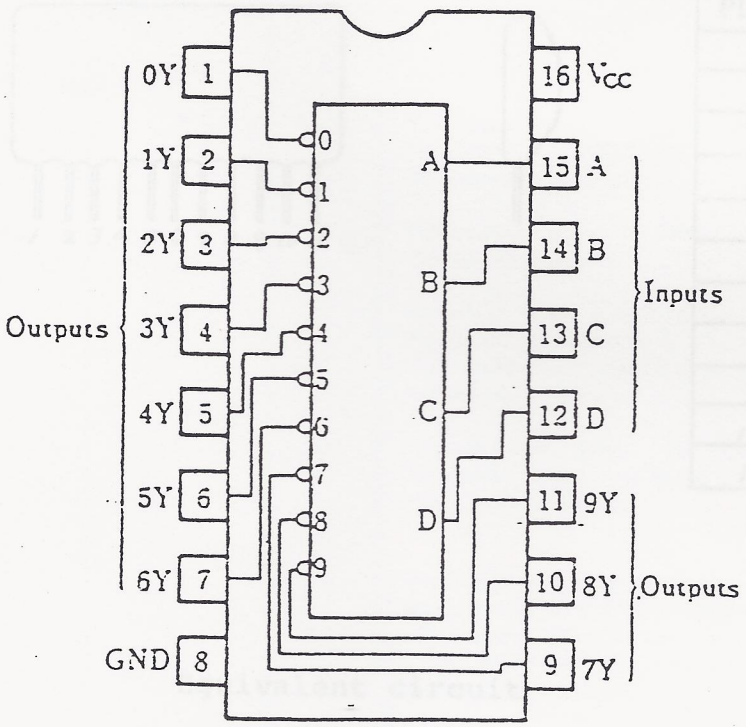
$D_0 \sim D_7$	:	Data bus (bidirectional)
$\overline{CS}$	:	Chip select
RESET	:	Reset
$\overline{RD}$	:	Read control
$\overline{WR}$	:	Write control
A_0 A_1	:	Port address
$PA_0 \sim PA_7$	:	I/O of port A
$PB_0 \sim PB_7$	:	I/O of port B
$PC_0 \sim PC_7$	:	I/O of port C

BLOCK DIAGRAM



(6) IC6: 74LS145

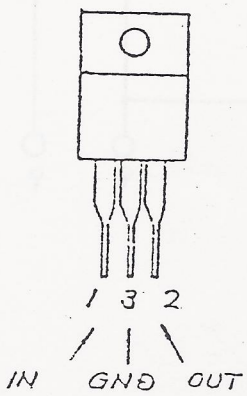
Terminal connection (Top View)



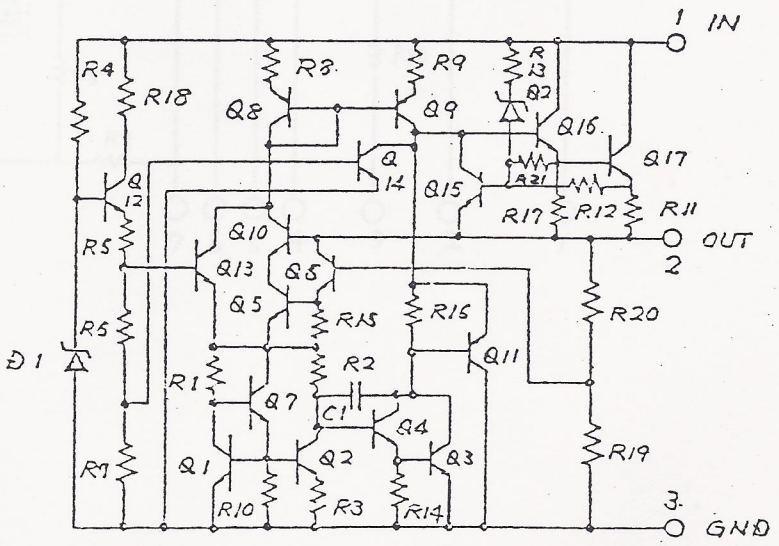
(7) IC7: PC7805

3-terminal regulator

Terminal connection

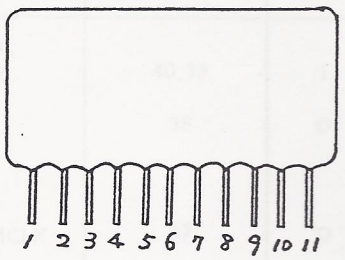


Equivalent circuit



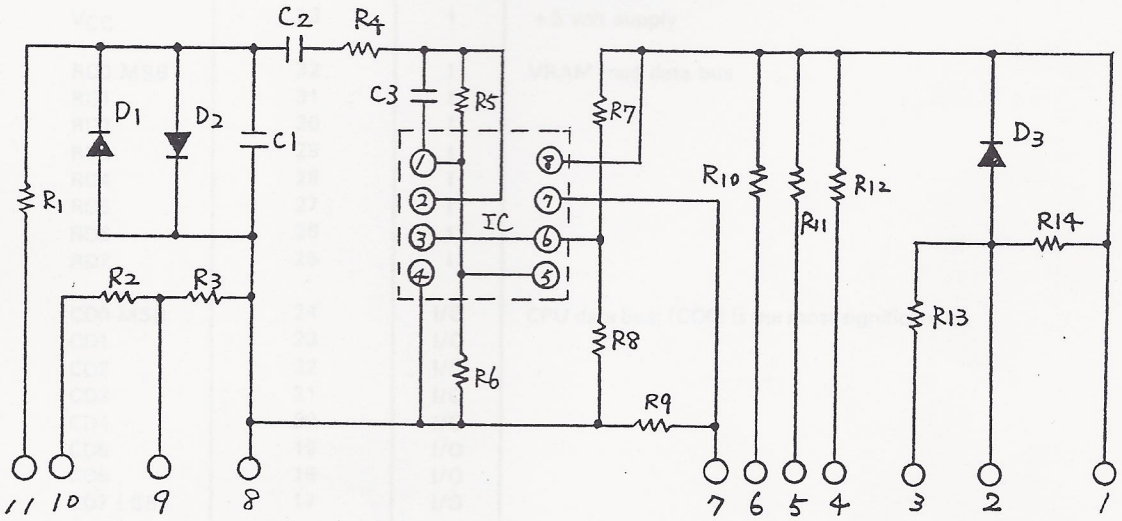
(8) IC8: Hybrid

Terminal connection



PIN No.	
1	+5V
2	N.C.
3	RESET
4	N.C.
5	N.C.
6	N.C.
7	IN
8	GND
9	MIC
10	OUT
11	EAR

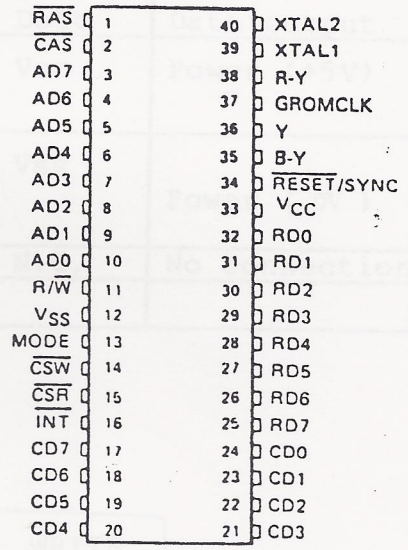
Equivalent circuit



(9) IC9 : TM9929A

TMS9928A/9929A Terminal Assignments

SIGNATURE	TERMINAL	I/O	DESCRIPTION
XTAL1, XTAL2	40,39	I	10.7 + MHz crystal inputs*
R-Y	38	O	VDP color burst frequency clock. On the TMS9928A/9929A, this is the R-Y color difference output.
GROMCLK	37	O	VDP output clock = XTAL/24. Typically not used.
Y	36	O	Composite video output. On the TMS9928A/9929A, this is the Y (black/white luminance and composite sync) output.
B-Y	35	I/O	External VDP input. On the TMS9928A/9929A, this is the B-Y color difference output.
$\overline{\text{RESET}}$/ SYNC	34	I	The $\overline{\text{RESET}}$ pin is a trilevel input pin. When it is below 0.8 volts, RESET initializes the VDP. When it is above 9 volts, RESET is the synchronizing input for external video.
V_{CC}	33	I	+5 volt supply
RD0 MSB	32	I	VRAM read data bus
RD1	31	I	
RD2	30	I	
RD3	29	I	
RD4	28	I	
RD5	27	I	
RD6	26	I	
RD7	25	I	
CD0 MSB	24	I/O	CPU data bus; (CD0) is the most significant bit
CD1	23	I/O	
CD2	22	I/O	
CD3	21	I/O	
CD4	20	I/O	
CD5	19	I/O	
CD6	18	I/O	
CD7 LSB	17	I/O	
$\overline{\text{INT}}$	16	O	CPU interrupt output.
$\overline{\text{CSR}}$	15	I	CPU-VDP read strobe
$\overline{\text{CSW}}$	14	I	CPU-VDP write strobe
MODE	13	I	CPU interface mode select; usually a processor address line

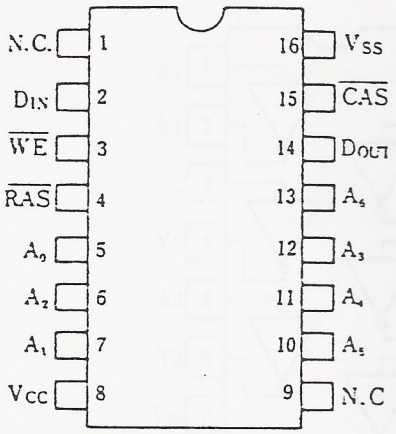


* When driven externally, both inputs must be driven.

** The least significant address bit (AD7) is wired to A0 of the dynamic RAMs. Likewise, AD6 is wired to A1 of the RAMs.

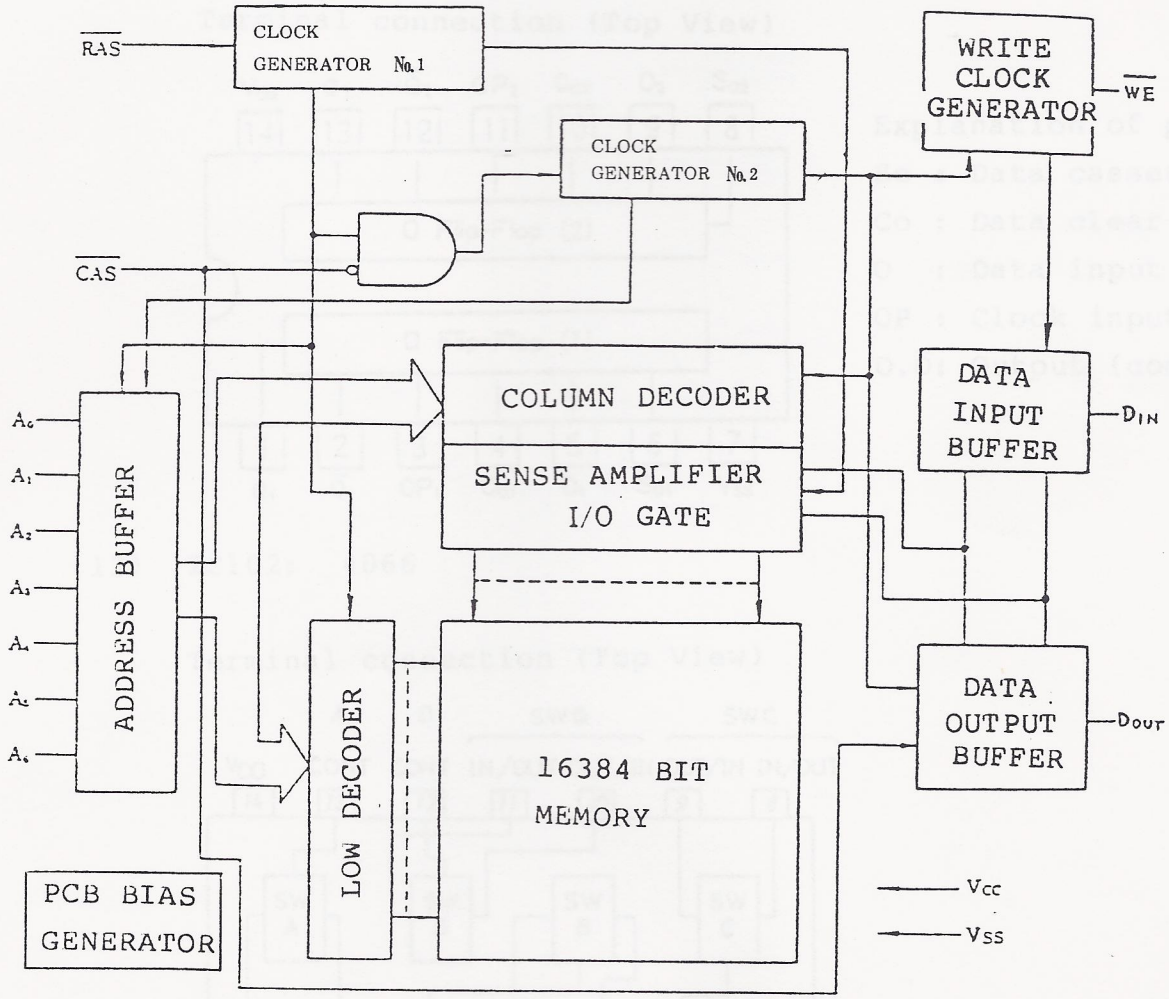
(10) IC10 IC17: 16K x 1 D-RAM

Terminal layout (Top View)



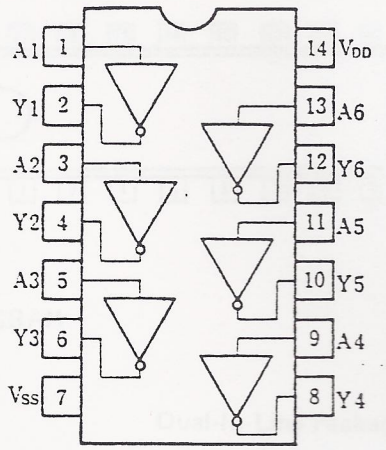
Symbols	Description of terminals	Symbols	Description of terminals
A0 ~ A6	Address	Dolt	Data output
RAS	Row address strobe	Vcc	Power (+5V)
CAS	Column address strobe	Vss	Power (0V)
WE	Write enable	N.C.	No connection
Din	Data input		

BLOCK DIAGRAM



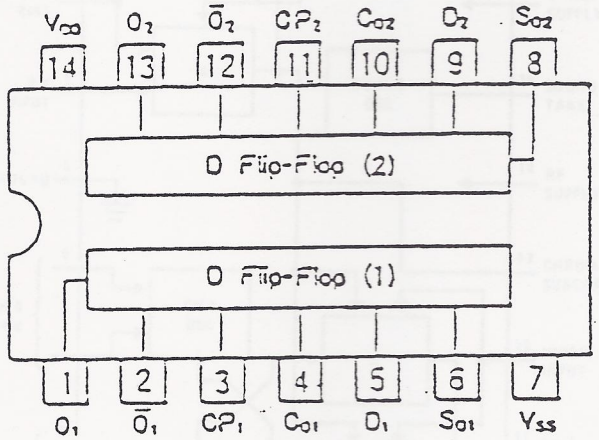
(11) IC18: 74HC04

Terminal connection (Top View)



(12) IC101 4013

Terminal connection (Top View)



Explanation of pins

So : Data cassette input

Co : Data clear input

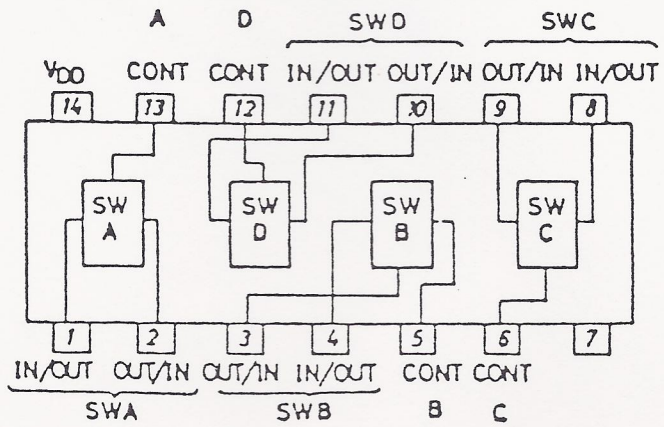
O : Data input

OP : Clock input

O.Ō: Output (complementary)

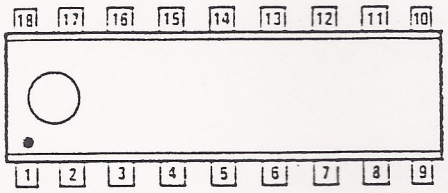
(13) IC102: 4066

Terminal connection (Top View)



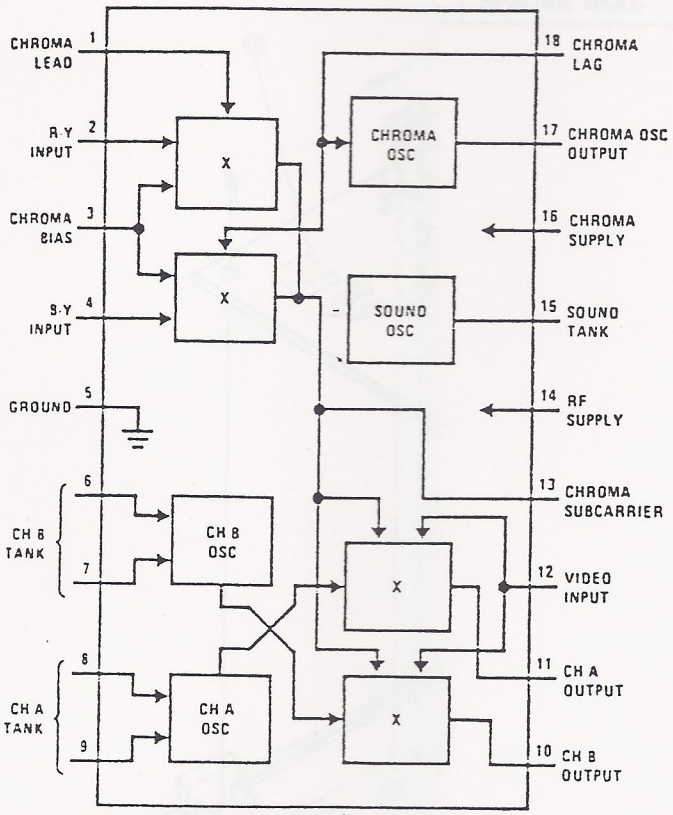
(14) IC103: LM1889

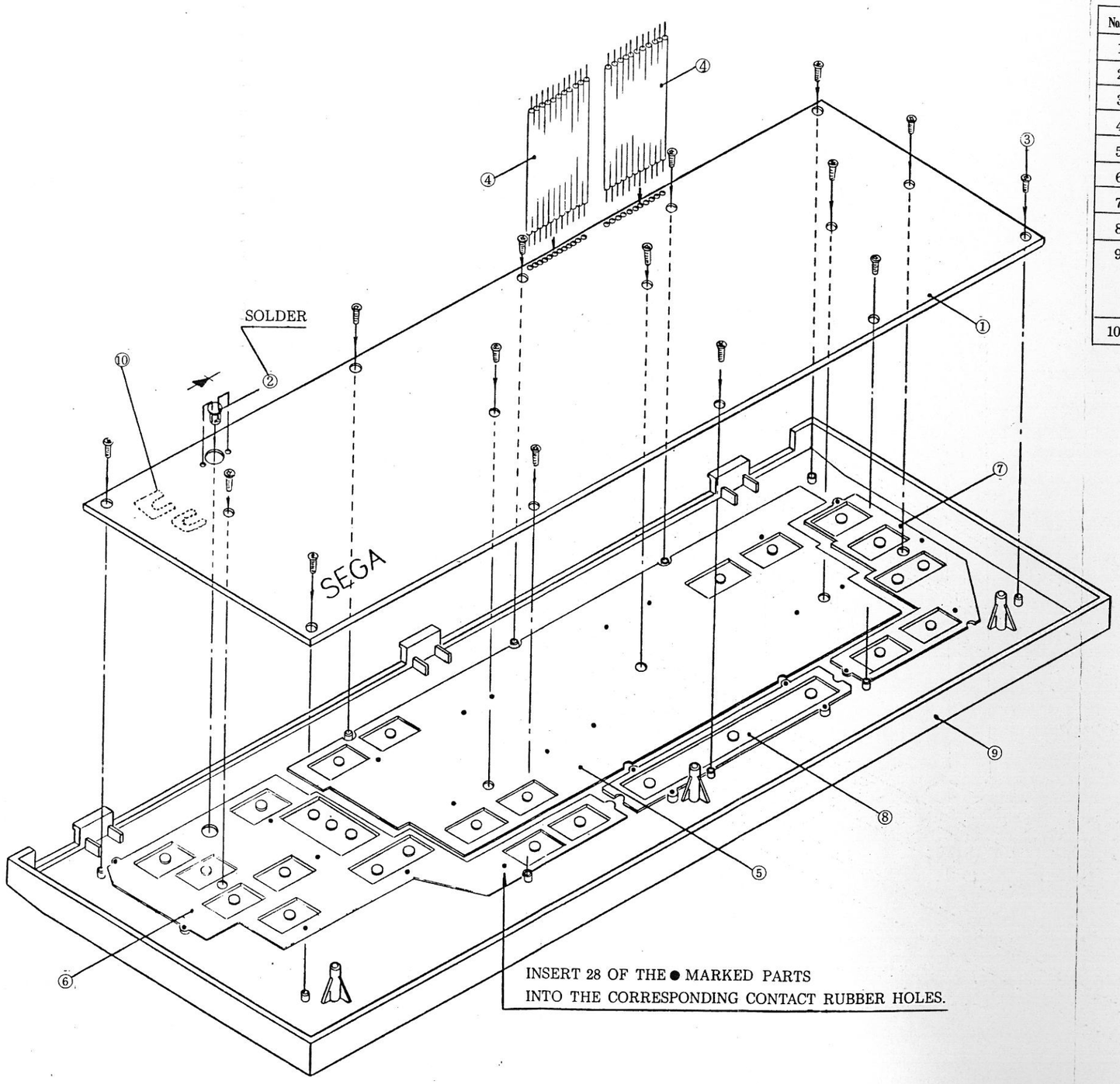
Terminal layout (Top View)



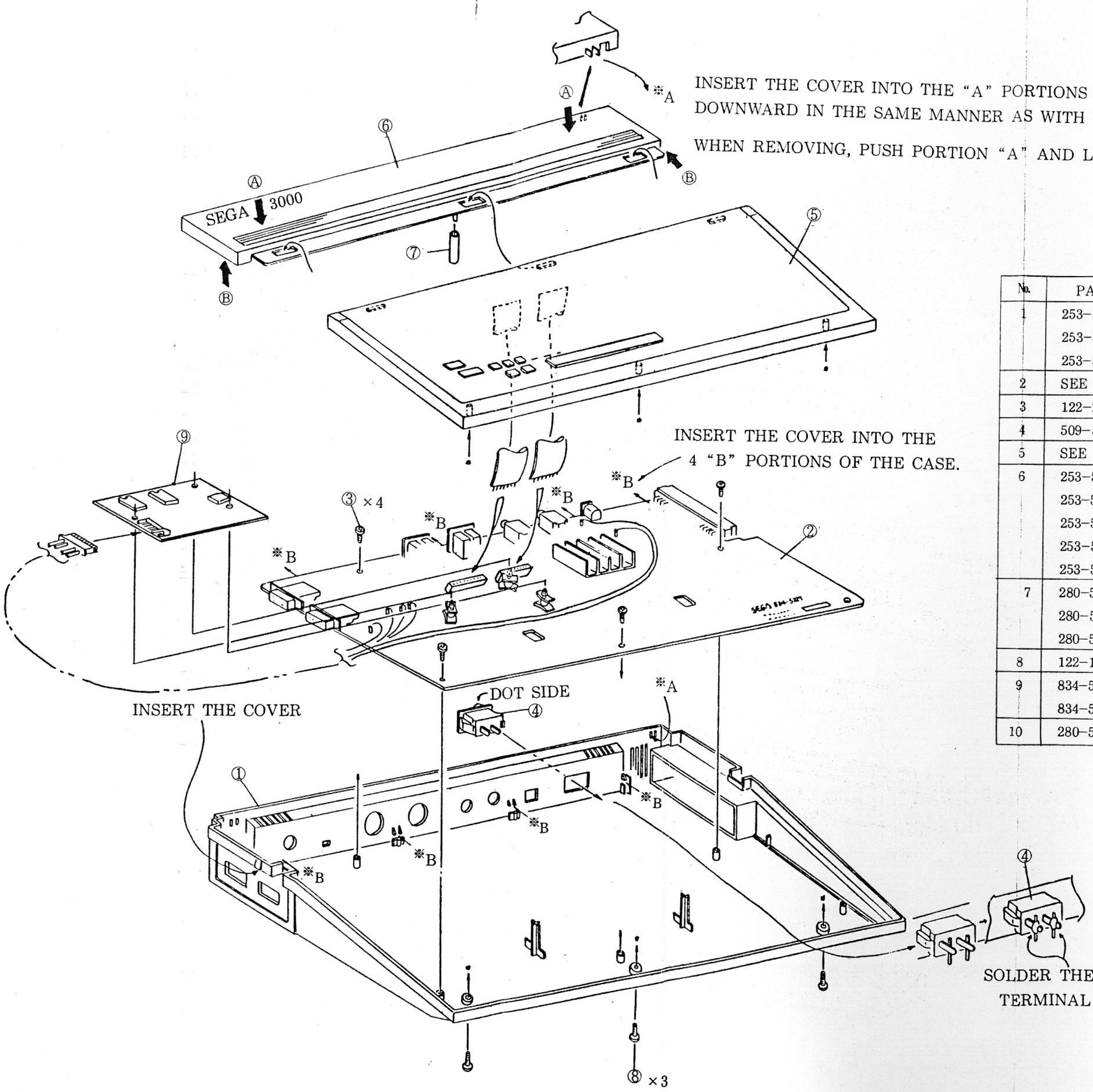
BLOCK DIAGRAM

Dual-In-Line Package

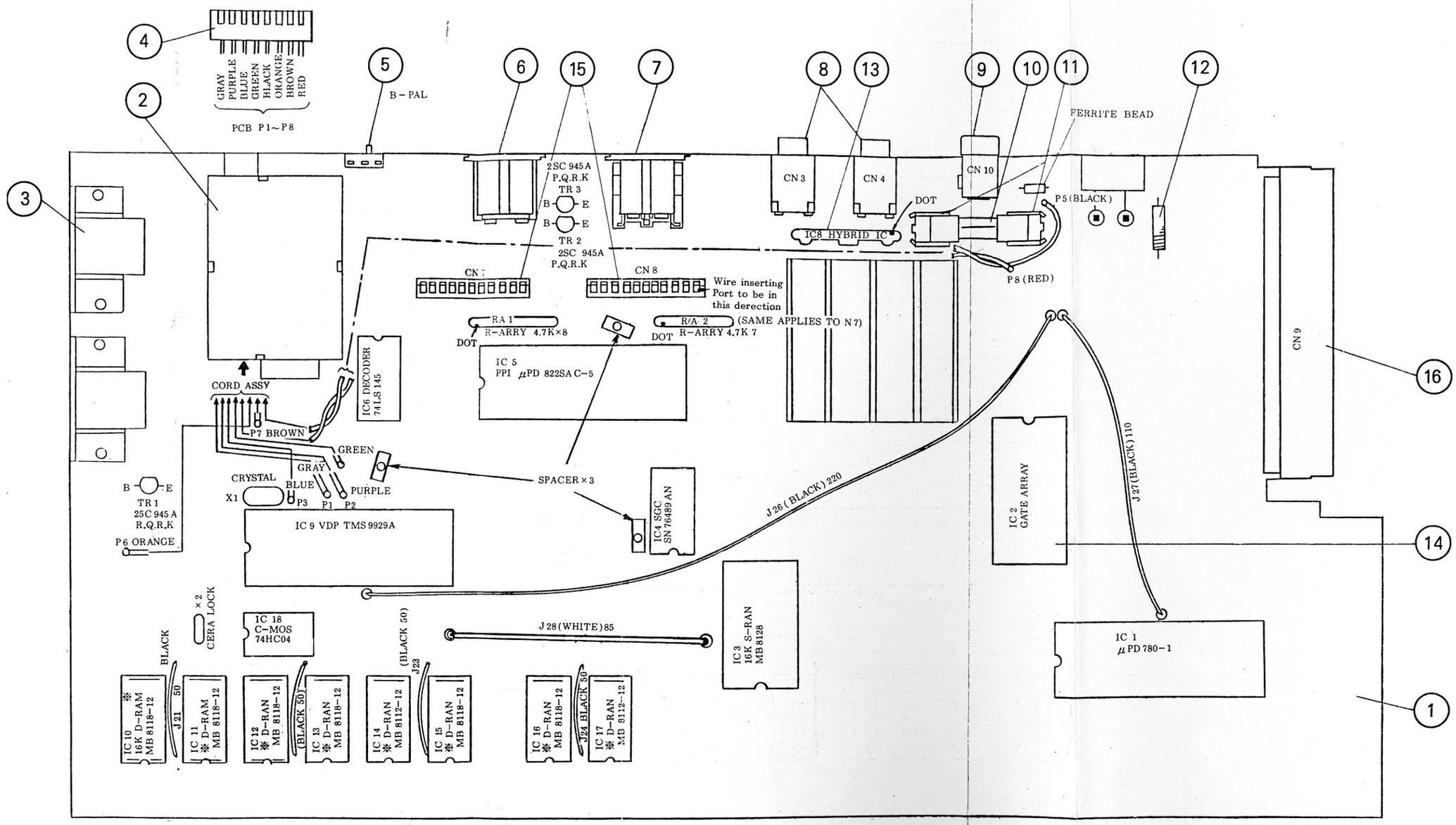


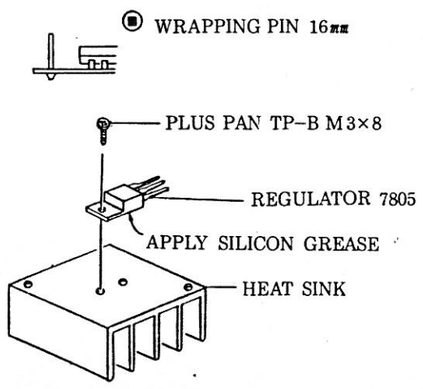


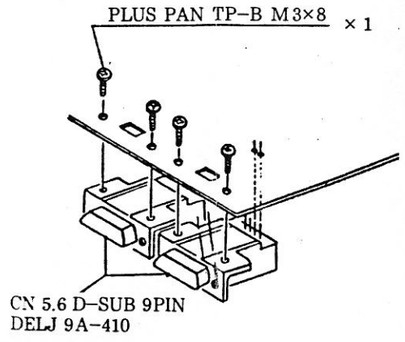
No.	PART No.	DESCRIPTION
1	171-5049	PC BOARD
2	390-5068	LED
3	122-211	TAPPING SCREW No.2 PH PHILL.2×5
4	600-5089	JUMPER WIRE 11P×80
5	509-5079	ASSY RUBBER CONTACT 1, 2 ETC. ENG.
6	509-5056	ASSY RUBBER CONTACT CR ETC.
7	509-5078	ASSY RUBBER CONTACT FUN ETC. ENG.
8	509-5057	ASSY RUBBER CONTACT SPACE
9	253-5022-B	KEYBOARD PANEL BLACK
	253-5022-I	KEYBOARD PANEL IVORY
	253-5022-R	KEYBOARD PANEL RED
10	601-5194	SPACER SEAL

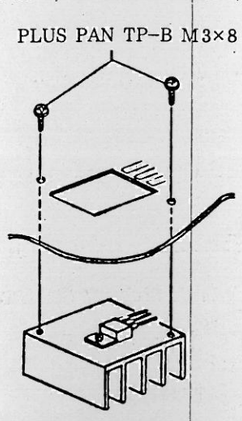


No.	PART No.	DESCRIPTION
1	253–5023–B	BOTTOM CASE BLACK
	253–5023–I	BOTTOM CASE IVORY
	253–5023–R	BOTTOM CASE RED
2	SEE PAGE 33	ASSY IC BOARD SC–3000
3	122–205	TAPPING SCREW No.2 PH PHILL 3×8
4	509–5062	POWER SWITCH
5	SEE PAGE 31	ASSY KEYBOARD
6	253–5022–B	KEYBOARD PANEL BLACK
	253–5022–I	KEYBOARD PANEL IVORY
	253–5022–R	KEYBOARD PANEL RED
	253–5022–HO	KEYBOARD PANEL HOME COMPUTER BLACK
	253–5022–YE	KEYBOARD PANEL YENO BLACK
7	280–5030–B	SPACER A BLACK
	280–5030–I	SPACER A IVORY
	280–5030–R	SPACER A RED
8	122–166	TAPPING SCREW No.2 PH PHILL 3×12
9	834–5482–01	ASSY IC BOARD R.G.B
	834–5483–01	ASSY IC BOARD PAL
10	280–5020	LOCKING SUPPORT


4
GRAY
PURPLE
BLUE
GREEN
BLACK
ORANGE
BROWN
RED
PCB P1~P8
2
5
B-PAL
6
15
7
8
13
9
10
11
12
FERRITE BEAD
3
2SC 945A
P.Q.R.K
TR 3
TR 2
2SC 945A
P.Q.R.K
CN 3
CN 4
CN 10
DOT
P5 (BLACK)
IC8 HYBRID IC
P8 (RED)
CN 7
CN 8
Wire inserting Port to be in this derection
RA 1
R-ARRY 4.7K×8
DOT
R/A 2
R-ARRY 4.7K 7
(SAME APPLIES TO N7)
IC 5
PPI μPD 822SA C-5
CN 9
16
CORD ASSY
IC6 DECODER
74LS 145
P7 BROWN
GREEN
GRAY
BLUE
PURPLE
CRYSTAL
X1
P3
P1
P2
SPACER × 3
B
E
TR 1
25C 945 A
R.Q.R.K
P6 ORANGE
IC 9 VDP TMS 9929A
IC4 SGC
SN 76489 AN
J26 (BLACK) 220
IC 2
GATE ARRAY
J27 (BLACK) 110
14
× 2
CERA LOCK
IC 18
C-MOS
74HC04
BLACK
J21
50
(BLACK 50)
J23
J28 (WHITE) 85
IC3
16K S-RAN
MB 8128
IC 1
μPD 780-1
1
IC 10
※
16K D-RAM
MB 8118-12
IC 11
※ D-RAM
MB 8118-12
IC 12
※ D-RAN
MB 8118-12
IC 13
※ D-RAN
MB 8118-12
IC 14
※ D-RAN
MB 8112-12
IC 15
※ D-RAN
MB 8118-12
IC 16
※ D-RAN
MB 8118-12
J24 (BLACK 50)
IC 17
※ D-RAN
MB 8112-12


WRAPPING PIN 16㎜
PLUS PAN TP-B M3×8
REGULATOR 7805
APPLY SILICON GREASE
HEAT SINK


PLUS PAN TP-B M3×8 × 1
CN 5.6 D-SUB 9PIN
DELJ 9A-410


PLUS PAN TP-B M3×8